CS323 – Exercises
Week 6
28 March 2019

Problem 1:
A computer system has a 36-bit virtual address space with a page size of 8KB, 4 bytes per page table entry and uses a single-level paging.

1. How many pages are in the virtual address space?
2. What is the maximum size of addressable physical memory in this system?

Problem 2:
An x86-64 computer has a page table size of 4096 bytes, its page size is the same. A page table entry takes 8 bytes. Its CPU implements 48 bits of virtual address space. A multi-level page table is used because each table must be contained within a page. How many levels are required?

Problem 3:
We have a 32-bit address space, 4KB page sizes and 2 levels of page tables with the bits arranged in the following way: d=12, p2=10, p1=10. Only the upper 10MB and lower 2MB are used. How many page table entries are required?

Problem 4:
The hardware for computer Dumbo was badly designed. The hardware designers included a valid bit in each page table entry, with the usual meaning, but they forgot to include a reference bit. Can you think of a way to implement a reference bit in software? You may assume that each page table entry has an unused bit field that you can read and write.

Problem 5:
A TLB has a hit rate of 95% and the TLB penalty T_{miss} = 150 cycles. Assume that, on a TLB hit, address translation takes T_{hit}=0. Compute the average time in cycles required for an address translation.