Design Technologies for Integrated Systems (Fall 2018-2019)

Master and PhD-level Depth Course for the IC and STI departments.

ECTS Credit Points: 6

Instructors:

- Lecturer: Prof. **Giovanni De Micheli** [giovanni dot demicheli at epfl dot ch]

- Assistant: **Eleonora Testa** [eleonora dot testa at epfl dot ch]

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Schedule:

- Tuesday 8:00-10:00, INM 10: Lecture

- Thursday 10:00-11:00, INF 119: Lecture

- Thursday 11:00-13:00, INF 119: Exercises

Objectives:

Students will learn the techniques used for designing integrated circuits and systems starting from design languages and formalism to the synthesis and optimization of digital circuits in terms of logic gates.

Content:

Hardware compilation is the process of transforming specialized hardware description languages into circuit descriptions, which are iteratively refined, detailed and optimized. The course will present the most outstanding features of hardware compilation, as well as the techniques for optimizing logic representations and networks. The course gives a novel, up-to-date view of digital circuit design. Practical sessions will teach students the use of current design tools.

Syllabus:

- Modeling languages and specification formalisms

- High-level synthesis and optimization methods (scheduling, binding, data-path and control synthesis)

- Representation and optimization of combinational logic functions (encoding problems, binary decision diagrams)

- Representation and optimization of multiple-level networks (algebraic and Boolean methods, "don't care" set computation, timing verification and optimization)

- Modeling and optimization of sequential functions and networks (retiming)

- Semicustom libraries and elements of physical design.

Prerequisites:

Logic design principles, Programming, Digital design

Textbook:

Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw-Hill, 1994.

A copy of the textbook can be borrowed (deposit of 50 CHF) at the secretary office: Carole Burget INF340

Grading :

Grades will be awarded on the basis of performance on tests, homework and mini-project. There will be homeworks covering exercises from the textbook. There will be a mini-project concerning VHDL and synthesis. The final grade for the course is the weighted sum of:

- Midterm exam: 20%

- Final exam: 35%

- Homeworks: 30%

- Mini-project: 15%

Teamwork:

Students may discuss in-between solutions of the homeworks but each student needs to individually write up a solution set. Students can be asked to explain their solutions during practical sessions.