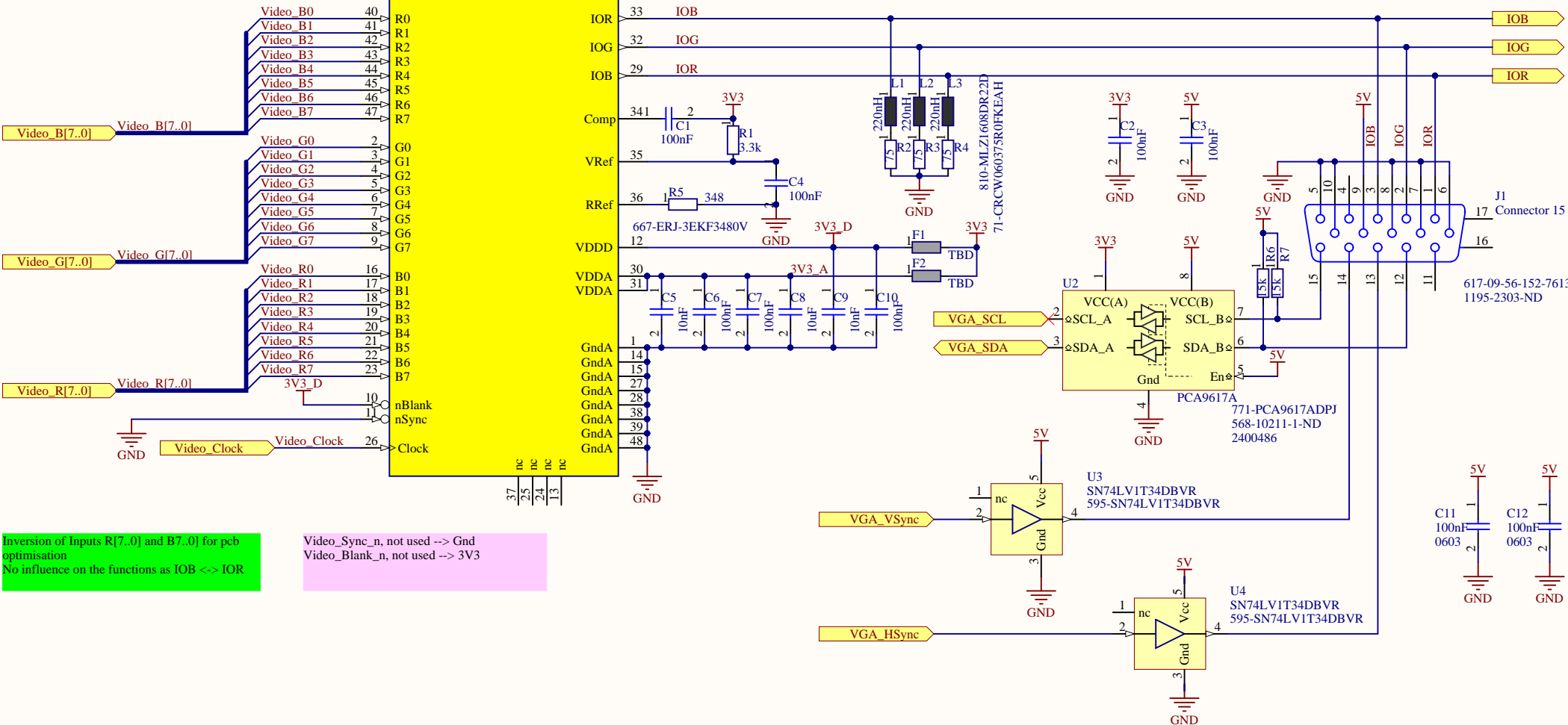


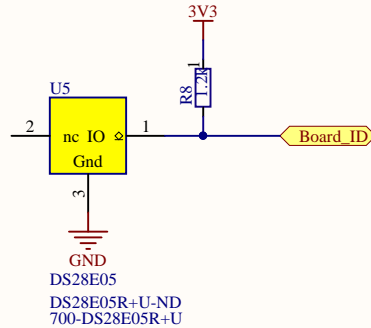
U1  
 CDK3404  
 939-CDK3404ATQ48

VGA connection  
 i2c @5V ??? R32/R33 for FPGA protection  
 Pull\_Up 15k on computer side  
 Only one master, read only access  
 Monitor address: 0x50 << 1 + R/nW -> 0xA1: 1010 0001  
 0x30 << 1 + 0 -> 0x60: 0110 0000 + page number (0..0x7F)



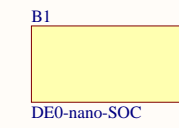
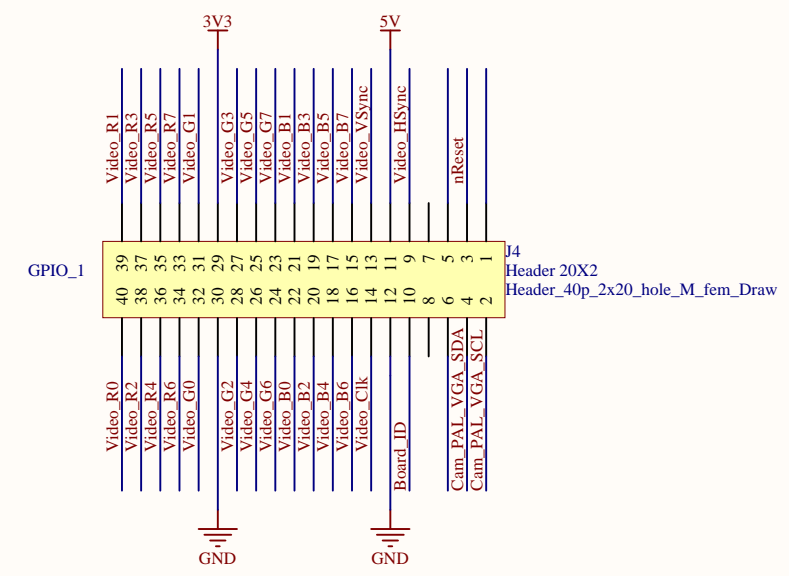
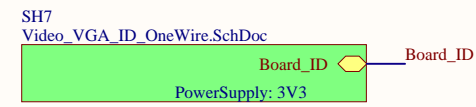
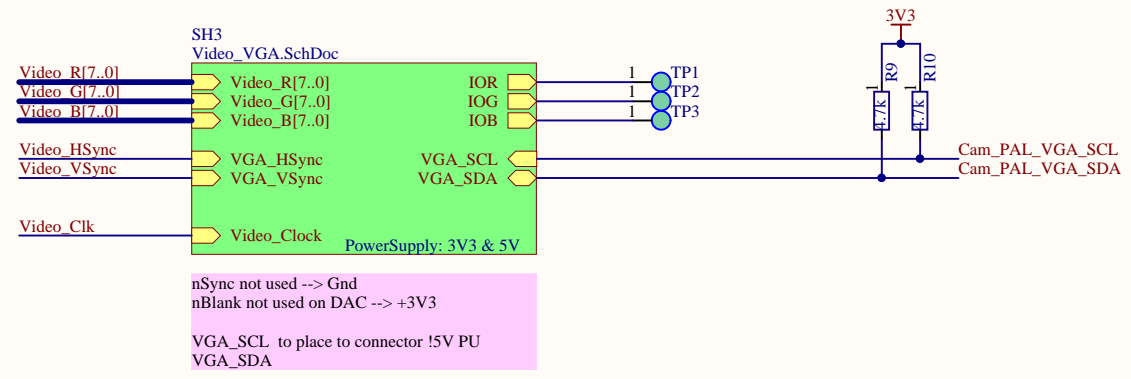
Inversion of Inputs R[7..0] and B[7..0] for pcb optimisation  
 No influence on the functions as IOB <> IOR

Video\_Sync\_n, not used -> Gnd  
 Video\_Blank\_n, not used -> 3V3



Title <b>Video_VGA_ID_OneWire</b>		* Video_VGA_ID_OneWire	
Size: A4	Number:*	Revision:*	R.Beuchat LAP/EPFL
Date: 29.09.2016	Time: 15:37:04	Sheet* of *	*
File: C:\Users\beuchatr\Dropbox\Developpements\PCB_Video_VGA\Video_VGA_ID_OneWire.SchDoc			





Title <b>Video_VGA_TOP</b>		* Video_VGA_TOP	
Size: A3	Number:*	R.Beuchat	
Date: 29.09.2016	Time: 15:37:04	EPFL/LAP	
File: C:\Users\beuchatr\Dropbox\Developpements\PCB_Video_VGA\Video_VGA_TOP.SchDoc		* * * *	





