$\frac{\text{Design Technologies for Integrated Systems} - \text{EPFL}}{\text{Exercise 8}} \\ \frac{29/11/2018}{}$

Problem 1

Consider the logic network defined as:

```
k=ad n=c+k m=(ab)' f=m+n Inputs are \{a,b,c,d\} and output is \{f\}. Assume CDC_{in}=ab. Compute CDC_{out}.
```

Problem 2

Consider the logic network above. Compute the ODC sets for all internal and input vertices assuming that the outputs are fully observable.