Design Technologies for Integrated Systems – EPFL

Homework 9 Assigned: 6/12/2018 Due: 13/12/2018

Problem 1

For the following functions:

$$\begin{aligned} F &= acde + acfg + bde + bfg + acd'h + bd'f \\ G &= acde + acf'g + bde + bf'g + aef' + ceh \end{aligned} \tag{1}$$

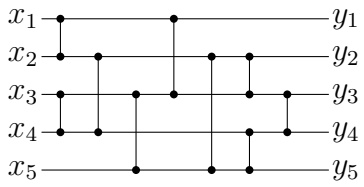
(a) Compute all kernels and co-kernels of F and G.

(b) Extract a multiple-cube sub-expression common to F and G.

(c) Draw the network graph using the result obtained in (b).

Problem 2

The smallest number of comparisons to sort 5 numbers is 9. One witness for this bound is the following sorter network:



The sorter network guarantees that $\{y_1, \ldots, y_5\} = \{x_1, \ldots, x_5\}$ and $y_1 \leq \cdots \leq y_5$.

1. Use this sorter network to construct an MIG that computes $\langle x_1 x_2 x_3 x_4 x_5 \rangle$.
2. How many majority-3 gates are required in a straightforward construction?

Problem 3

Consider the logic network defined as:
$c = (a + b)'$; $d = ab'$; $e = (ab)'$; $f = (ae)'$; $g = (be)'$;
$o_1 = c + d$; $o_2 = (fg)'$; $h = o_1 \oplus o_2$;.

(a) Draw the logic network graph.

(b) Write the Tseytin encoding for all gates in the network.

(c) Write the CNF formula that can be used to check the equivalence of subnetworks o_1 and o_2.

Problem 4

Consider the logic network defined as:

$k = a'$; $e = kb$; $g = (bc)'$; $f = (g + e')$;

$h = a \odot b$; $i = f \oplus d$; $j = d + s$; $x = ei$; $y = (h + j)'$.

Inputs are $\{a, b, c, d, s\}$ and outputs are $\{x, y\}$.

Assume that NAND, NOR, XOR, XNOR delay is 2 unit and AND, INV, OR delay is 1 unit. The date ready time of signal d is 4 ($t_d = 4$) The data ready time of other signals is 0. The required data time at outputs is 7.

(a) Draw the logic network graph.

(b) Determine the data ready time and the slacks for all nodes.

(c) Find the topological critical paths.

(d) Are the topological critical paths statically/dinamically sensitizable?

Problem 5

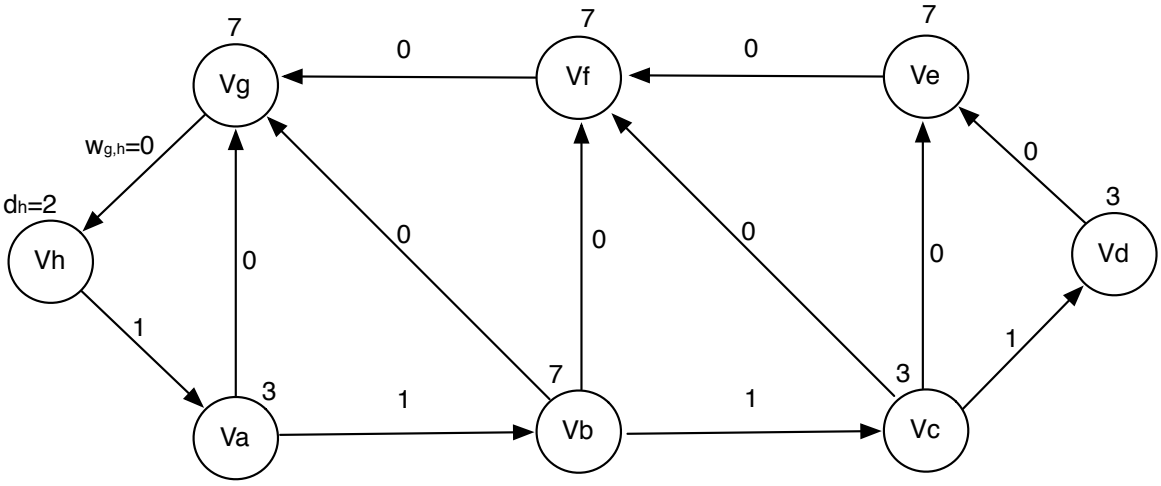


Figure 1: Sequential logic network

Consider the sequential logic network G(V,W,d) in Fig. 1. Each vertex represents a combination logic circuit, whose weight corresponds to its logic delay. The weight of each edge corresponds to the number of registers between two vertices.

(a) Draw the constraint graph modeling to search for a legal retiming with a cycle-time of 17 units.

(b) Use Bellman-Ford method to find the retiming factor with the constraint graph.

(c) Compute the retiming vector **r** and redraw the retimed network graph.