Some synchronization problems with logic in FPGA

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DFF.. Sampling of input signals

Problem to solve:

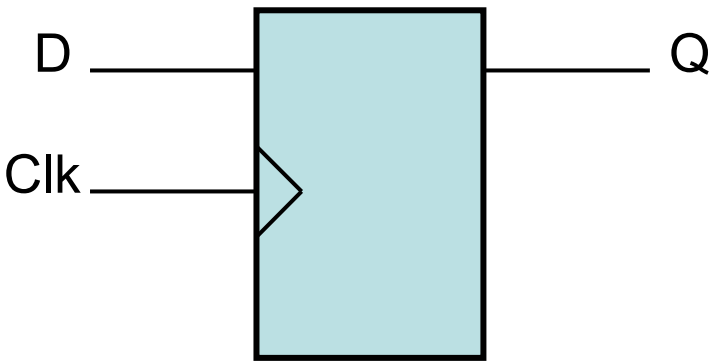
- If an external asynchronous signal is used inside a synchronous system it needs to be synchronized before use. Why ?
  1. Metastability problem
  2. At the same clk sampling time (i.e. rising_edge(Clk)), all the logic elements using this signal and clocking it, need to see it at the same logical level !!

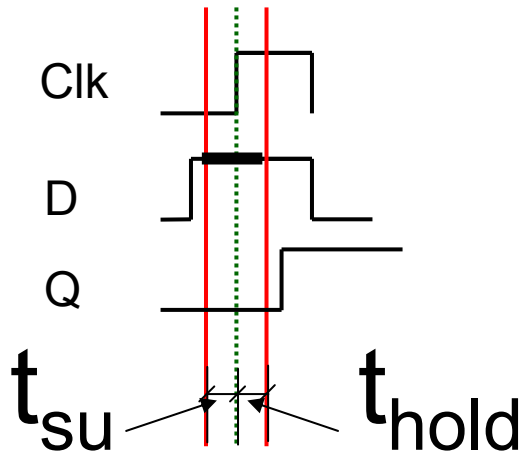
DFF.. Sampling of input signals

Metastability problem:

To be correctly sampled by a FF (Flip-Flop or D-register) a signal (D) needs to respect 2 very important timings:

- ***t_{su}: Set up time: D valid before ↑Clk***
- ***t_{hold}: Hold time: D stay valid after ↑Clk***



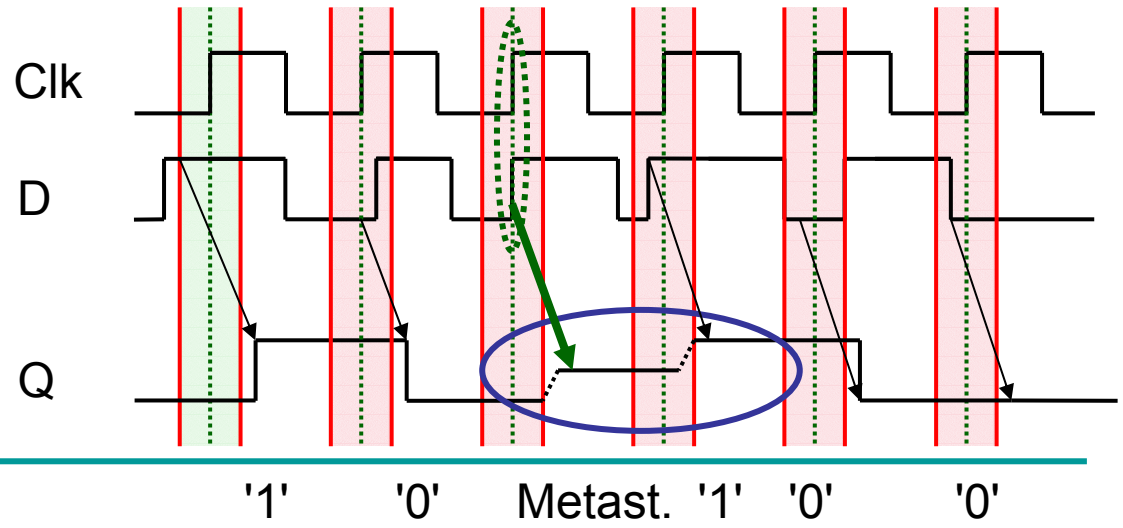


DFF.. Sampling of input signals

If the rule is NOT respected:

- *The output can be '0' or '1' → good*
- *The output can be in an intermediate level for an undefined time →* ***metastable*** *level*

The values sampled in the red area are not guarantied for their output value



DFF.. Sampling of input signals

- The level of the metastable signal is between the '0' and the '1'.
- The time the metastable signal stays is probabilistic and theoretically could be infinitive. Practically it disappears at the next signal sampling.
- Usually a DFF sampling a metastable level would not propagate it. As for this intermediate level, a decision is take for a '0' or a '1'.
- It could propagate to a next DFF if the level change just at the sampling point to the metastable threshold, the probability is very low but not 0 !
- Thus depending on the hardness of the design to do, more DFF are needed.

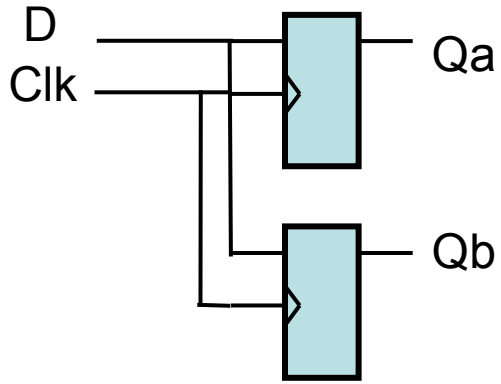
Manufacturer provides information about the parameters for metastability.

DFF.. Sampling of input signals

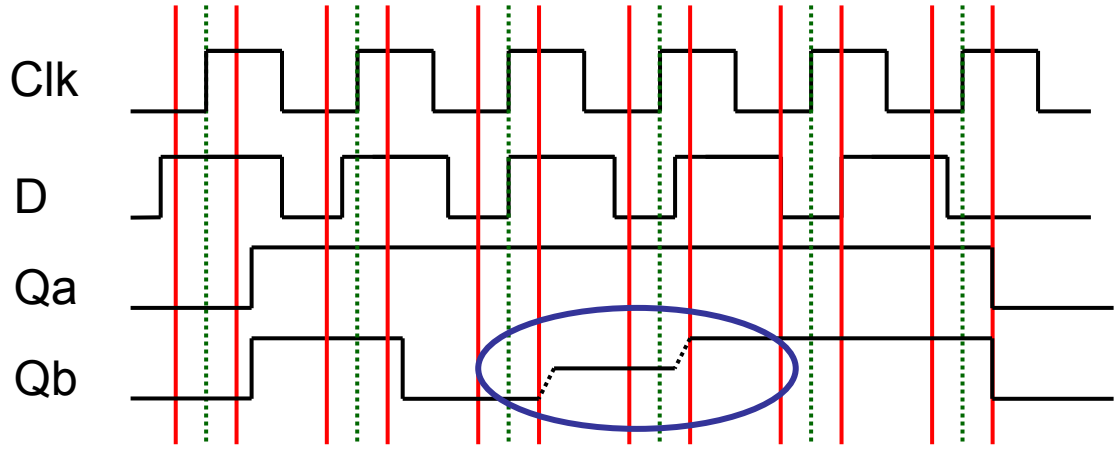
View of the same value for all the sampling FF.

If the rule is NOT respected:

- *Very bad for 1 DFF → worst if the same signal D is going to more than 1 DFF:*
- *each DFF could see a different input level*



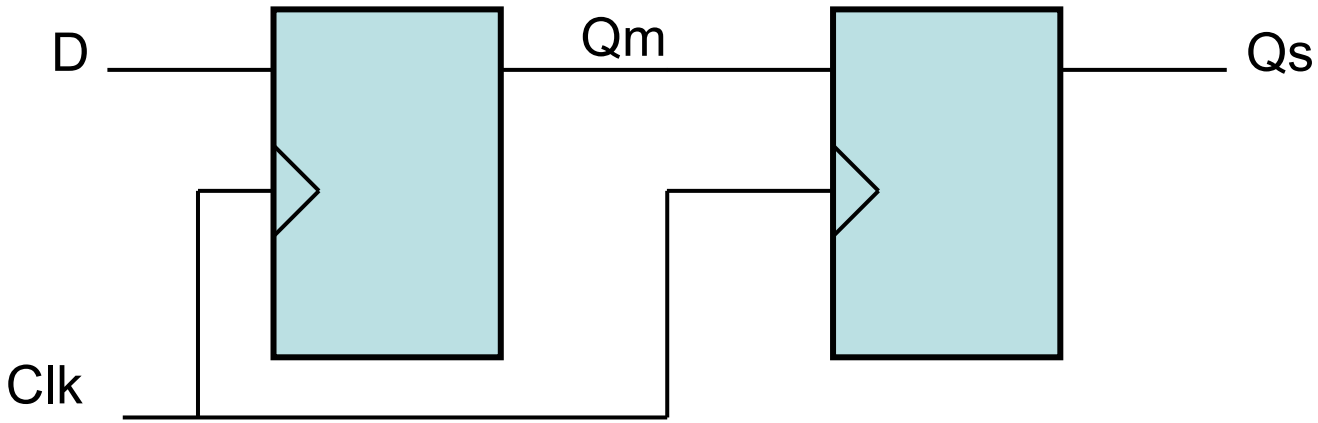
Qa, Qb :
2 different DFF outputs



DFF.. Sampling of input signals

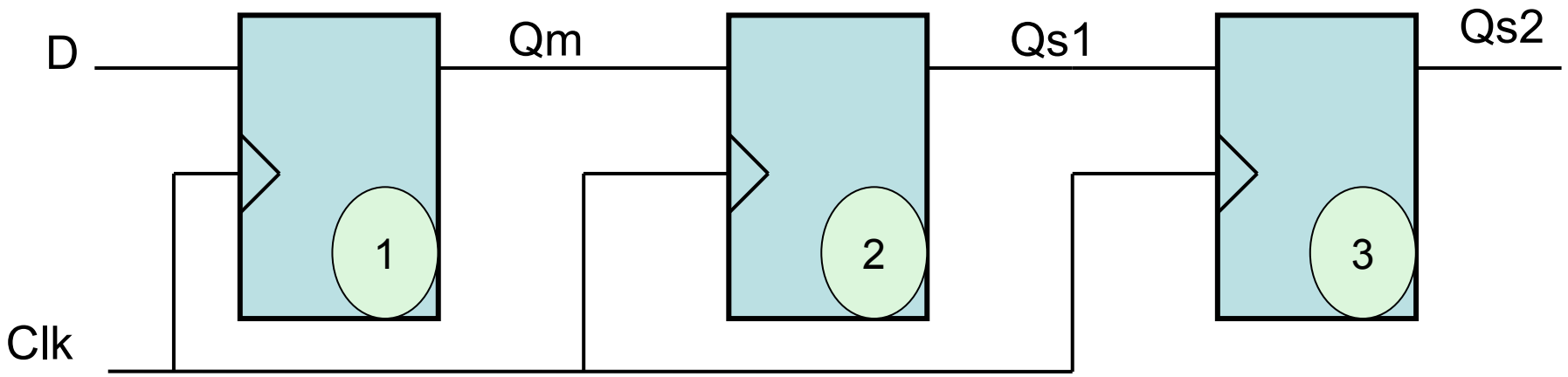
→At the same clk sampling time (i.e. rising_edge), all the logics using the signal and clocking it, need to see it at the same logic level !!

→A synchronizing system is necessary



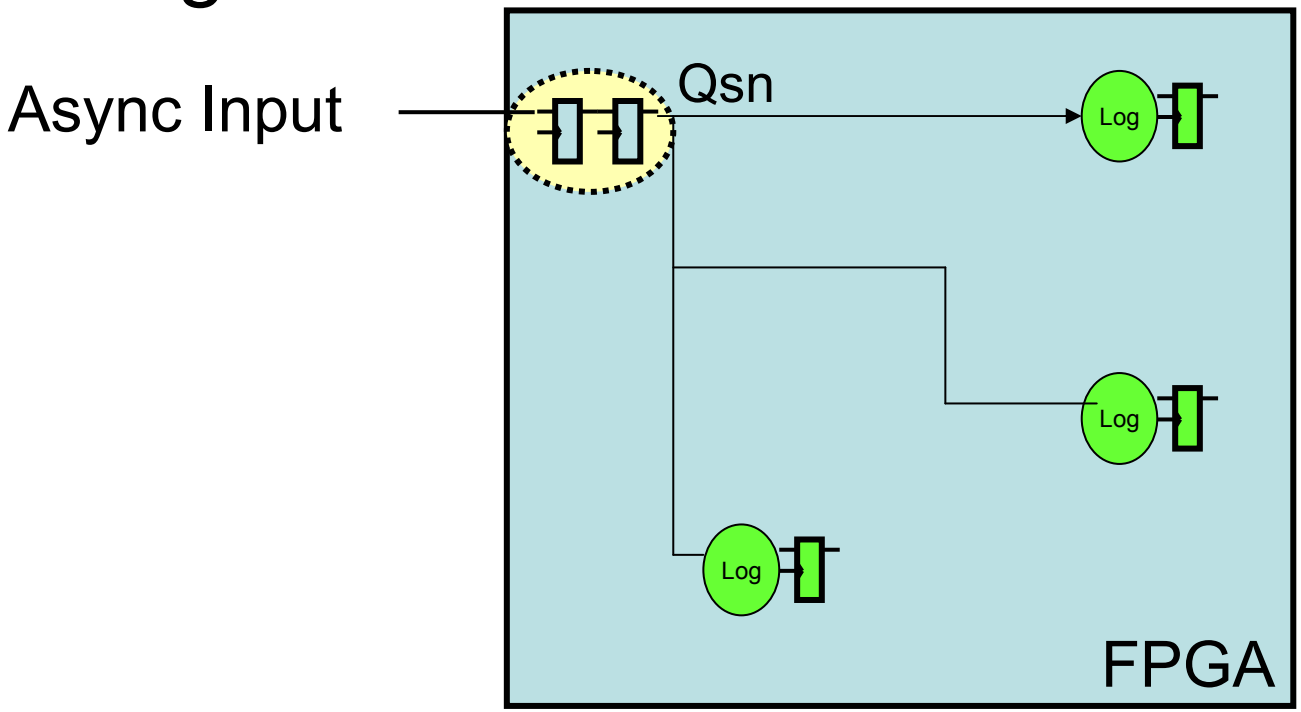
DFF.. Sampling of input signals

- → The first DFF can have a metastable signal as output Qm
- → The second one will **probably** filter it
- → For very high reliability system more DFF could be necessary, delay added !!



DFF.. Sampling of input signals

→ The Qsn signal can be used by all the logic that need it: the level will be the same for all the logic elements



DFF.. Sampling of input signals

Clock distribution

→ Inside the FPGA all the DFF using the same D signal need to use the same Clock.

→ Special global lines are available inside a FPGA for that purpose.

→ They are limited in number

→ If we expect to use a normal signal as a clock for a FF → it's a very bad idea

→ We need to use the **Clock Enable** feature of a DFF in a FPGA

DFF.. Conclusion

- → Asynchronous signals need to be synchronized before use in a FPGA
- → A simple DFF can generate metastable output
- → At least a second DFF is necessary to filter this metastable signal