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Nanoscale MOSFET Modeling

Part 2: Using the inversion coefficient as the primary design parameter

This article illustrates the use of the *inversion coefficient* (*IC*) as the main design parameter to explore the various tradeoffs faced in the design of analog circuits. We start with showing that the same transconductance, gain-bandwidth (GBW) product, or input-referred thermal noise resistance of a common-source (CS) amplifier can be achieved with lower current by shifting the IC toward moderate inversion (MI) at the cost of a slight increase of the transistor aspect ratio and area. In such case the self-loading gate capacitance cannot be ignored, and accounting for it introduces a minimum bias current at an IC that lies in the middle of the MI to achieve a given GBW.

Various figures-of-merit (FoMs) are then introduced starting with the current or transconductance efficiency G_m/I_D. It is shown that G_m/I_D is maximum in weak inversion (WI) and that because of velocity saturation (VS) more current is required in strong inversion (SI) to reach the same transconductance than when VS is absent. The transit frequency F_t is then derived as a function of the IC, and it is shown that it reaches a maximum $F_{t\text{peak}}$ in SI that is inversely proportional to the VS parameter λ_c. It is also shown that $F_{t\text{peak}}$ does not scale as $1/L$ and only depends on the ratio of the oxide capacitance per unit area to the total extrinsic gate capacitance per unit width. Finally the product $G_m/I_D \cdot F_t$ FoM is introduced. The latter reaches a maximum in MI, offering a good tradeoff among gain, noise, and current consumption. All the presented FoMs can be expressed versus the IC using simple analytical expressions requiring only four parameters. They are favorably compared to measurements of short-channel devices from 40- and 28-nm bulk CMOS technologies and with the BSIM6 compact model for the 40-nm device, illustrating the effectiveness of using the IC in the design of analog circuits.

Introduction

The design of analog circuits is the art of finding the right tradeoff between conflicting constraints or specifications such as power, noise,

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linearity, gain, supply voltage, voltage swing, speed and input/output impedance, as illustrated by Razavi's analog design octagon, shown in Figure 1 [1]. After having found the most appropriate system architecture and circuit, the designer finally needs to select the right drain bias current, channel width, and length for each metal–oxide–semiconductor (MOS) transistor [2]. These three independent degrees of freedom for each device influence their performance, including bias voltages, dc gain, bandwidth, noise, matching, and linearity and hence have an impact on the overall circuit performance [2].

Among all the transistor parameters (current, width, length, and bias voltages), the overdrive voltage $V_G - V_{T0}$ has been used as a key design variable for a long time. However, with the down-scaling of complementary MOS (CMOS) technology, the operating points of MOS transistors have been progressively pushed toward moderate or even WI (subthreshold region), where the overdrive voltage is not convenient anymore. To cover the whole range of operating regimes from WI to SI, we propose replacing the overdrive voltage by the IC describing the state of inversion of the channel from weak via moderate to SI.

The concept of IC was introduced in the first part of this article [3], together with the simplified charge-based Enz–Krummenacher–Vittoz (EKV) MOS field-effect transistor (FET) model that can be used to model devices in saturation even in advanced CMOS processes with only a few parameters including the effect of VS. The model includes simple expressions of the normalized (source) *transconductance* and the *transconductance efficiency* G_m/I_D in terms of *IC* and the VS parameter λ_c. Similarly, the output conductance in saturation for short-channel devices can also be expressed in terms of *IC* and two additional parameters λ_d and σ_d. The model was validated on several advanced bulk and fully depleted silicon on insulator (FDSOI) CMOS processes [3].

In this second part, we will investigate how this simplified EKV model can be used to explore the various tradeoffs faced when designing analog circuits. Since much circuit performance directly depends on G_m and/or G_{ds}, it can be characterized over a wide range of bias using the expressions of G_m and G_{ds}.

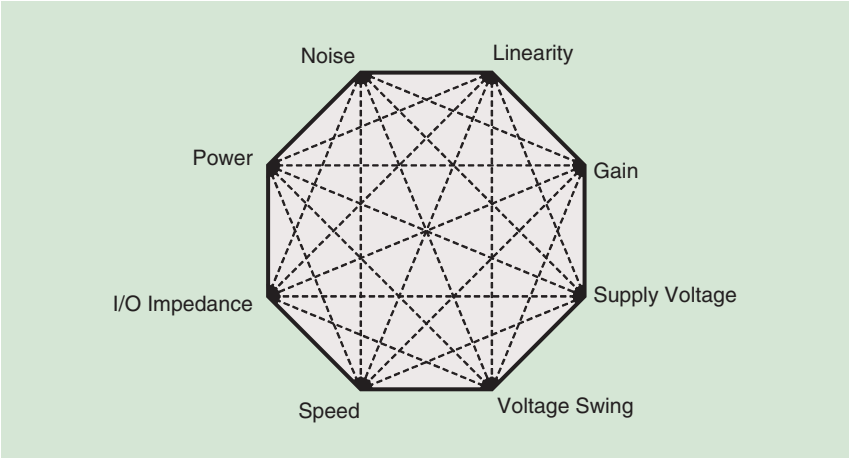

FIGURE 1: Razavi's analog design octagon, illustrating the tradeoffs faced in the design of analog circuits [1].

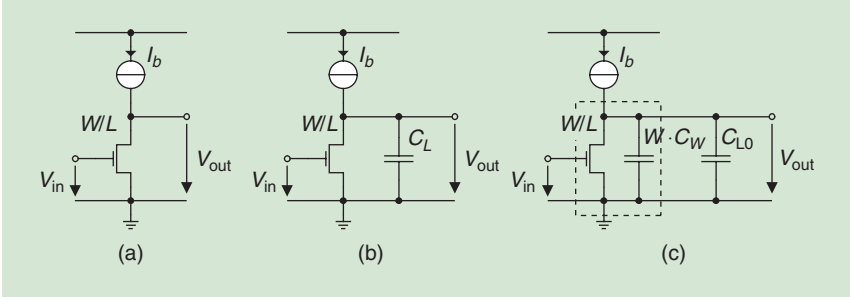

FIGURE 2: CS gain stage schematics for the calculation of (a) constant G_m, (b) constant *GBW*, and (c) constant *GBW* including self-loading.

Basic Tradeoffs in Analog IC Design

The transconductance, and hence the current and area, of a single-stage amplifier or a differential pair is often dictated by the requirements on gain, GBW product, and noise [4], [5]. Because the transconductance is proportional to the aspect ratio W/L and increases with the current, the same transconductance can be achieved for different W/L ratios and bias current. Hence, the designer still has the degree of freedom to choose the appropriate *IC* at which the device needs to be biased to achieve a given transconductance. It will be shown below that moving the operating point to MI or WI actually comes with a reduction of current at the cost of an increase in area to achieve the same transconductance, GBW, or input-referred thermal noise [4], [5]. To show this, we will look at the simple CS stage shown in Figure 2. We will investigate how the bias current I_b and aspect ratio W/L of a transistor

varies with IC for a given G_m, GBW, and input-referred thermal noise resistance R_n.

Constant-G_m

The transconductance of an MOS transistor such as in the CS gain stage shown in Figure 2(a) is proportional to the transistor aspect ratio W/L and depends on the bias current I_b. The latter can be reduced to lower the power consumption, but the aspect ratio has to be increased to achieve the same transconductance, therefore increasing the transistor area. This tradeoff between the bias current and the transistor aspect ratio can be explored by means of the IC using the definition of the normalized source transconductance $g_{ms}(IC)$ given in [3]. The gate transconductance G_m can be written as

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC), \tag{1}$$

where W and L are the width and length of the transistor, n is the slope factor, and $U_T \triangleq kT/q$ is the thermodynamic voltage [3]. $I_{spec\square} \triangleq 2n\mu_0 C_{ox} U_T^2$ is the *specific current per square*, which is a fundamental parameter for a given technology and type of transistor (n- or p-channel), where μ_0 is the low field mobility in the channel region and C_{ox} the oxide capacitance per unit area [3]. g_{ms} is the normalized source transconductance given by [3]

$$g_{ms} \triangleq \frac{G_{ms}}{G_{spec}} = \frac{n \cdot G_m}{G_{spec}} = \frac{\sqrt{(\lambda_c IC + 1)^2 + 4IC} - 1}{\lambda_c(\lambda_c IC + 1) + 2}, \tag{2}$$

where $G_{spec} \triangleq I_{spec}/U_T = 2n\mu_0 C_{ox} U_T$ and $\lambda_c \triangleq L_{sat}/L$ is the VS parameter corresponding to the fraction of the channel in which the carrier drift velocity reaches the saturated velocity v_{sat} over a portion of the channel length $L_{sat} = 2\mu_0 U_T / v_{sat}$ [3].

From the definition of IC given in [3], the drain current in saturation can be written as

From this perspective, MI turns out to be a good tradeoff between low current and acceptable area for achieving a given transconductance.

$$I_D = I_{spec} \cdot IC = I_{spec\square} \cdot \frac{W}{L} \cdot IC. \tag{3}$$

Solving (1) and (3) for I_D and W/L results in

$$I_D = I_b = \frac{G_m \cdot nU_T \cdot IC}{g_{ms}(IC)}, \tag{4a}$$

$$\frac{W}{L} = \frac{G_m \cdot nU_T}{g_{ms}(IC) \cdot I_{spec\square}}, \tag{4b}$$

which can be normalized to the desired transconductance G_m according to

$$i_b \triangleq \frac{I_b}{G_m \cdot nU_T} = \frac{IC}{g_{ms}(IC)}, \tag{5a}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{I_{spec\square}}{G_m \cdot nU_T} = \frac{1}{g_{ms}(IC)}. \tag{5b}$$

The normalized bias current i_b and aspect ratio AR are plotted in Figure 3 for different values of the VS parameter λ_c. It shows that the same G_m can be achieved with lower current by shifting IC toward MI and WI where i_b saturates to unity. This is obtained at the cost of a significant increase of the transistor aspect ratio (or of the transistor width W for a fixed length L) resulting in a drastic area increase. From this perspective, MI turns out to be a good tradeoff between low current and acceptable area for achieving a given transconductance [4], [5].

Constant Gain-Bandwidth Product

An important specification that determines the transconductance of single-stage amplifiers as the CS amplifier shown in Figure 2(b) is the GBW product GBW or unity-gain frequency ω_u given by

$$\omega_u = \frac{G_m}{C_L} = \omega_L \cdot \frac{W}{L} \cdot g_{ms}, \tag{6}$$

where C_L is the load capacitance at the drain of the transistor and $\omega_L \triangleq I_{spec\square}/(nU_T C_L)$ is a normalizing quantity corresponding actually to the GBW of a square transistor biased in WI. If C_L is assumed to be constant, then (6) and (3) can be solved for I_D and W/L and normalized to the desired GBW, resulting in

$$i_b \triangleq \frac{I_b}{I_{spec\square}} \cdot \frac{1}{\Omega} = \frac{IC}{g_{ms}}, \tag{7a}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{1}{\Omega} = \frac{1}{g_{ms}}, \tag{7b}$$

where $\Omega \triangleq \omega_u/\omega_L$. Note that this normalization leads to the same expressions for i_b and AR as in (5a) and (5b), which are plotted in Figure 3. Again, for achieving a given GBW product, current can be saved by moving the operating point toward MI at the cost of a slight increase in

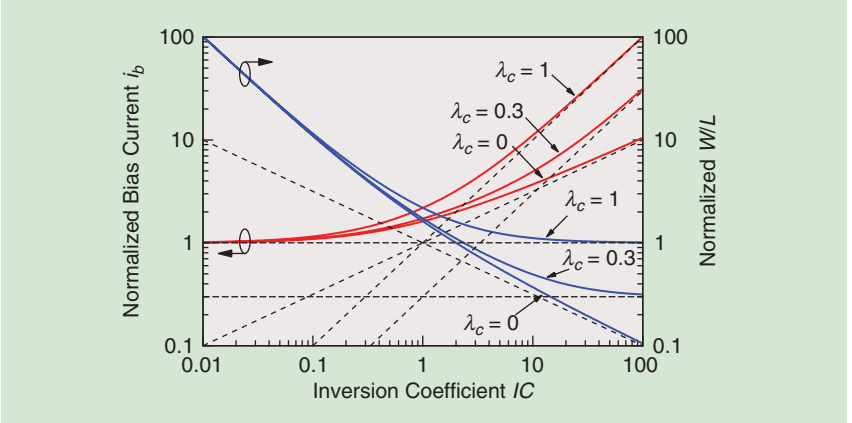

FIGURE 3: The normalized current and W/L ratio versus IC for a constant G_m and GBW.

transistor width. Moving it further toward WI does not gain much current and costs a lot of area [4], [5].

The assumption that the load capacitance remains constant becomes obviously erroneous as the transistor gets wider. Indeed, since the parasitic capacitance of the transistor is proportional to the width W, enlarging the transistor to move the operating point to WI makes this parasitic capacitance contribute significantly to the load capacitance at the drain. This can be accounted for as illustrated in Figure 2(c) by splitting the load capacitance into a constant part C_{L0} (typically including the wire capacitance and the capacitance of the next stage) and a part that scales proportionally to the transistor width W

$$C_L = C_{L0} + C_w \cdot W, \tag{8}$$

where C_w is the self-loading capacitance per unit width mostly due to overlap and fringing field capacitances. Equations (6) and (3) can then be solved for i_b and W/L accounting for (8), resulting in the following normalized current and aspect ratio [6]–[8]:

$$i_b \triangleq \frac{I_D}{I_{spec\square}} \cdot \frac{1}{\Omega} = \frac{IC}{g_{ms} - \kappa\Omega}, \tag{9a}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{1}{\Omega} = \frac{1}{g_{ms} - \kappa\Omega}, \tag{9b}$$

where $\kappa \triangleq C_w L / C_{L0}$ is the ratio of the self-loading parasitic capacitance of a square transistor ($W = L$) to the fixed load capacitance. Equations (9a) and (9b) are plotted versus IC for a constant GBW ($\Omega = 0.1$) in Figure 4(a) without accounting for VS ($\lambda_c = 0$) [6], [8]. It shows that the current accounting for self-loading ($\kappa = 0.3$ and $\kappa = 1$) now reaches a minimum for an optimum IC given by

$$IC_{opt} = 2\kappa\Omega(1 + \kappa\Omega) + \sqrt{\kappa\Omega(1 + \kappa\Omega)(1 + 2\kappa\Omega)^2}. \tag{10}$$

This is because when reducing IC and at the same time increasing W leads to an increase of C_L and hence a reduction of ω_u that has to be compensated by an increase of the current to maintain ω_u constant. The curves in Figure 4(a) are without accounting for VS. Figure 4(b) shows i_b and AR for $\kappa = 0.3$ and for different values of λ_c. As expected, the impact of VS is negligible in WI whereas the required current to achieve the same GBW in SI gets significantly larger with VS. Notice that the optimum IC corresponding to the minimum current i_b when VS is present is no more given by (10) and cannot be solved analytically, but (10) can still be used as a first guess since IC_{opt} is actually not much affected by VS as shown in Figure 4(b) [7], [8].

Constant Input-Referred Thermal Noise

The transconductance can also be determined by the input-referred thermal noise resistance R_n given by [9]

$$R_n = \frac{\gamma_{nD}}{G_m} = \frac{nU_T}{I_{spec\square} \cdot W/L} \cdot \frac{\gamma_{nD}}{g_{ms}}, \tag{11}$$

where $\gamma_{nD} \triangleq G_m R_n$ is the noise excess factor, which is slightly bias dependent for a long-channel transistor and is typically comprised between $n/2$ in WI and $2n/3$ in SI. For short-channel devices γ_{nD} raises quickly in SI due to several short-channel effects but usually stays lower than 3 [9]. It can be approximated as [10]

$$\gamma_{nD} \cong 1 + \alpha_\gamma \cdot IC \tag{12}$$

with $\alpha_\gamma \cong 0.07$ [10]. Solving (11) and (3) for I_D and W/L and normalizing to the desired R_n results in

$$i_b \triangleq \frac{I_D \cdot R_n}{nU_T} = \frac{\gamma_{nD} \cdot IC}{g_{ms}}, \tag{13a}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{R_n \cdot I_{spec\square}}{nU_T} = \frac{\gamma_{nD}}{g_{ms}}. \tag{13b}$$

The normalized bias current i_b and aspect ratio AR given by (13) are plotted versus IC in Figure 5 for different values of λ_c and α_γ. It shows that the required current for achieving a given R_n in SI is significantly larger in case of a short channel device where both λ_c and α_γ are different than zero. Moderate inversion is again a sweet spot for a balanced tradeoff between current consumption and area for achieving a given input-referred thermal noise.

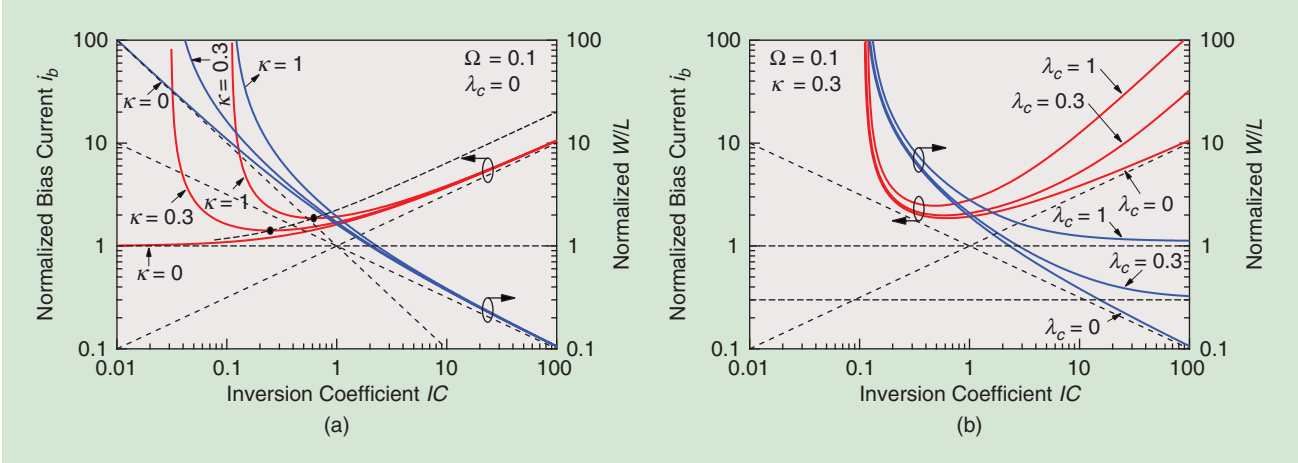

FIGURE 4: The normalized current and W/L ratio versus IC for a constant GBW including self-loading capacitance: (a) without VS ($\lambda_c = 0$) and (b) including VS.

The next section will show how some FoMs can be used as design guidelines using IC as the main variable to help designers choosing the appropriate region of operation for reaching their specs at the lowest power.

FoMs as Design Guidelines

The Transconductance Efficiency G_m/I_D

The transconductance efficiency G_m/I_D FoM is one of the most important performance metrics for analog circuit design. It is a measure of how much transconductance is produced for a given bias current and is a function of IC. The transconductance efficiency (or its inverse) appears in many expressions related to the power optimization of analog circuits. We actually already have seen it (or the inverse) in expressions (5), (7), and (13), derived, respectively, for constant G_m, constant ω_u, or constant R_n.

In the normalized form, the transconductance efficiency is defined as the actual gate transconductance obtained at a given IC with respect to the maximum transconductance $G_m = I_D/(nU_T)$ reached in WI [7]

$$\frac{g_{ms}}{IC} = \frac{G_m \cdot nU_T}{I_D} = \frac{\sqrt{(\lambda_c IC+1)^2+4IC}-1}{IC\cdot[\lambda_c\cdot(\lambda_c IC+1)+2]}. \quad (14)$$

The expression in (14), which is continuous from WI to SI and includes the effect of VS, is plotted in Figure 6. The figure shows the behavior of g_{ms}/IC for long-channel devices in which VS is absent which scales as $1/\sqrt{IC}$ in SI (dashed blue curve). For short-channel devices subject to VS, the drain current becomes a linear function of the gate voltage, independent of the transistor length. Hence, the transconductance becomes independent of the current and length. Since G_m becomes independent of I_D or IC, the G_m/I_D curve scales like $1/(\lambda_c IC)$ in SI instead of $1/\sqrt{IC}$ when VS is absent. In essence, the effect of VS is to degrade the transconductance efficiency in SI, meaning that more current is required to reach the same transconductance obtained without VS. Nevertheless, irrespective of the channel length, G_m/I_D remains invariant (i.e., $g_{ms}/IC = 1$) in WI, since short-channel effects, including VS, have the same effect on G_m than on I_D simply because G_m is proportional to I_D in WI.

The Transit Frequency F_t

The transit frequency F_t is defined as the frequency at which the extrapolated small-signal current gain of the transistor in CS configuration falls to unity [9]. F_t is a widely used metric for characterizing the high-frequency behavior of a MOSFET because many performances, such as the gain at RF and the minimum noise factor, are directly linked to F_t [9]. A good approximation of F_t is given by [9], [11]

$$F_t = \frac{G_m}{2\pi C_G}, \quad (15)$$

where $C_G = C_{Gi} + C_{Ge}$ is the total gate capacitance comprising the *intrinsic capacitance* C_{Gi}, which is linked to the mobile charges in the channel, and the *extrinsic capacitance* $C_{Ge} = C_{GeW}\cdot W$, including the overlap and fringing field capacitances as shown in Figure 7, which scale with the transistor width W. Since both G_m and C_{Gi}, are bias dependent, F_t is bias dependent too. Its variation with respect to IC is shown in Figure 8. In WI, the mobile charges are few and the intrinsic gate capacitance is negligible compared to the extrinsic capacitance so that $C_G \cong C_{Ge}$. The bias dependence in WI is mostly coming from G_m. Since in WI $G_m \propto I_D$

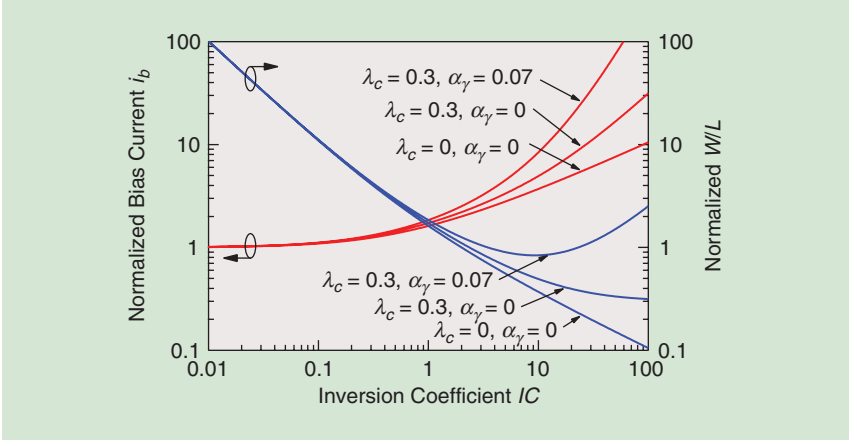

FIGURE 5: The normalized current and W/L ratio versus IC for a constant input-referred thermal noise resistance R_n.

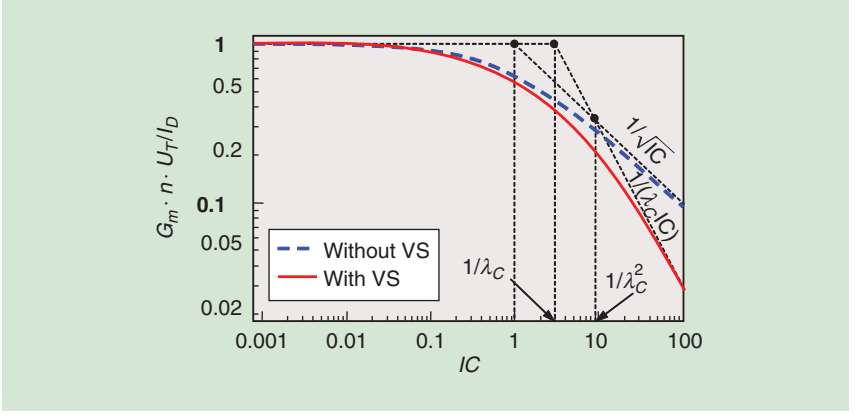

FIGURE 6: g_{ms}/i_d versus IC showing the long and short channel asymptotes.

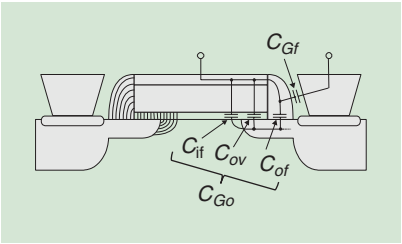

FIGURE 7: The extrinsic gate capacitances made of the overlap capacitance C_{Go} and the fringing field capacitance C_{Gf}.

and hence $G_m \propto IC$, F_t is therefore also proportional to IC.

Similarly to G_m/I_D, F_t can be normalized as shown in Figure 8 to F_{tspec} defined as the value of F_t on the WI asymptote corresponding to $IC = 1$ [12]. In this way, the normalized transit frequency $f_t \triangleq F_t/F_{tspec}$ turns out to be equal to g_{ms}, which is given by (2). Note that F_{tspec} scales roughly as $1/L$ [12]

$$F_{tspec} = F_{spec} \cdot \frac{WLC_{ox}}{C_G} \cong F_{spec} \cdot \frac{WLC_{ox}}{C_{Ge}} = \frac{I_{spec\square}}{2\pi n U_T C_{GeW} L}, \quad (16)$$

where $F_{spec} \triangleq 2\mu_0 U_T/(2\pi L^2)$.

As illustrated in Figure 8, in SI and under VS (i.e., for $1/\lambda_c^2 < IC$), F_t (or ft in normalized form) saturates to F_{tspec}/λ_c (or $1/\lambda_c$ in normalized form). When increasing the channel length, i.e., for lower values of λ_c, the value of F_t at which VS starts, moves to higher values and there is a region between $IC = 1$ and $IC = 1/\lambda_c^2$ where F_t follows the SI asymptote $\sqrt{IC}$.

Note that once the VS parameter is extracted from the G_m/I_D as described in [3], it is therefore easy to assess the peak F_t for a given technology from F_{tspec}. It is also interesting to point out that the denormalized value of the saturation value of F_t is given by [12]

$$F_{tpeak} = \frac{F_{tspec}}{\lambda_c} = \frac{WC_{ox}v_{sat}}{2\pi C_G} \cong v_{sat} \cdot \frac{C_{ox}}{2\pi C_{GeW}}, \quad (17)$$

which shows that, surprisingly, F_{tpeak} does not scale as $1/L$ anymore [12]. This means that the only way to increase F_{tpeak} is to increase C_{ox} but without increasing C_{GeW} [12]. This observation could explain the recent slow down of the peak transit frequency progression witnessed in recent years.

The $G_m/I_D \cdot F_t$ FoMs

Both G_m/I_D and F_t are very important FoMs from an analog/RF design perspective: the former characterizes the dc performance of a device while the latter characterizes its high-frequency performance. However, as is clear from Figures 6 and 8, there exists a fundamental tradeoff between the two. Aiming for low-power operation by targeting a high G_m/I_D at small values of IC invariably means compromising in speed (bandwidth). This is where the FoM defined as the product of the two formerly defined metrics comes into the picture. Combining two quantities that have their maxima on the opposite ends of the IC axis, the $G_m/I_D \cdot F_t$ FoM [13] serves as design guide to locate the optimum IC.

It can be justified from the small-signal voltage gain of the CS stage shown in Figure 9, which is given by

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{G_m Z_L}{1 + \omega R_S C_{GS}} \cong -\frac{\omega_u}{\omega}, \quad (18)$$

where $\omega_u = \omega_t \cdot Z_L/R_S$ is the unity-gain frequency and G_m/C_{GS} has been approximated by the transit frequency ω_t. It can be shown that the noise factor NF, neglecting the noise of the bias current source, is given by

$$NF = 1 + \frac{\gamma_{nD}}{G_m R_S}. \quad (19)$$

An FoM can be defined such that it maximizes the unity gain bandwidth ω_u while minimizing the added noise $NF - 1$ and the bias current I_b

$$\text{FoM}_{RF} \triangleq \frac{\omega_u}{(NF-1)\cdot I_b} = \frac{Z_L}{R_S \cdot \gamma_{nD}} \cdot \frac{G_m \cdot \omega_t}{I_b}, \quad (20)$$

which is proportional to the product of G_m/I_b and F_t. Neglecting the bias dependence of γ_{nD}, this product can be expressed in terms of IC using the normalized $G_m/I_D \cdot F_t$ FoM defined as [7]

$$\text{fom}_{rf} \triangleq \frac{g_{ms} \cdot f_t}{IC}, \quad (21)$$

where $f_t \triangleq g_m/c_g$ is the normalized transit frequency with $g_m \triangleq G_m/G_{spec}$ and $c_g \triangleq C_G/(WLC_{ox})$. As shown in

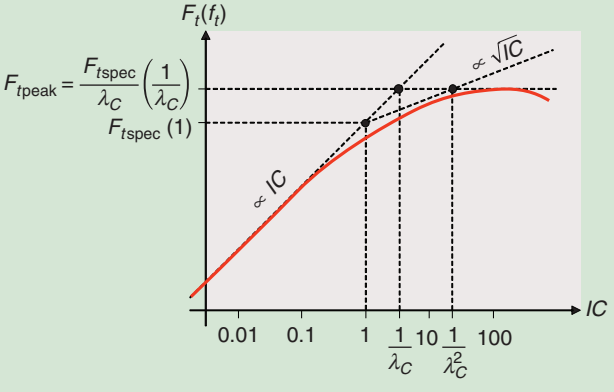

FIGURE 8: The transit frequency F_t versus IC showing the definition of F_{tspec}. The variables in parenthesis correspond to the normalized transit frequency.

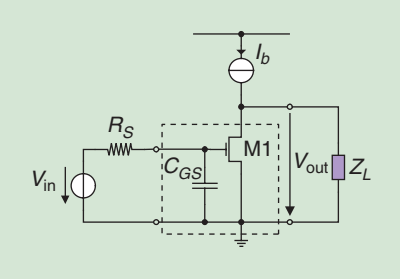

FIGURE 9: The CS amplifier used for derivation of the $G_m/I_D \cdot F_t$ FoM.

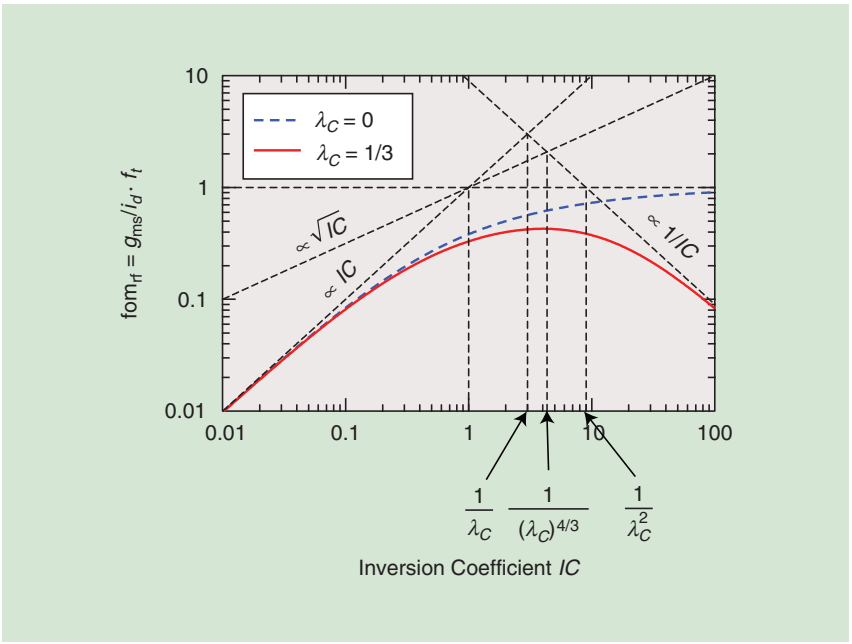

FIGURE 10: The normalized FoM fom_{rf} (on a log scale) as a function of IC, along with the WI and SI asymptotes. The peak of the FoM lies at the intersection of IC and $1/(\lambda_c^2 IC)$ asymptotes.

Figure 10, fom_{rf} shows a peaking behavior [13] that makes it useful for locating the optimum IC, which is due to the asymptotic behavior of two quantities that it incorporates [7], [14]. This maximum is located approximately at $IC \cong 1/\lambda_c^{4/3}$. What is even more interesting is that this peak lies at the higher end of the MI region for the contemporary CMOS technologies and moves deeper into the MI region with decreasing channel lengths, as shown in the bottom plot of Figures 11 and 12. It is worth noting that the peaking behavior of this FoM is caused by the degradation of G_m and G_m/I_D in SI due to VS [14]. In the absence of VS, in SI, G_m (consequently F_t) and G_m/I_D are respectively proportional to $\sqrt{I_D}$ and $1/\sqrt{I_D}$, implying that the FoM would simply saturate in this region as shown by the blue dashed

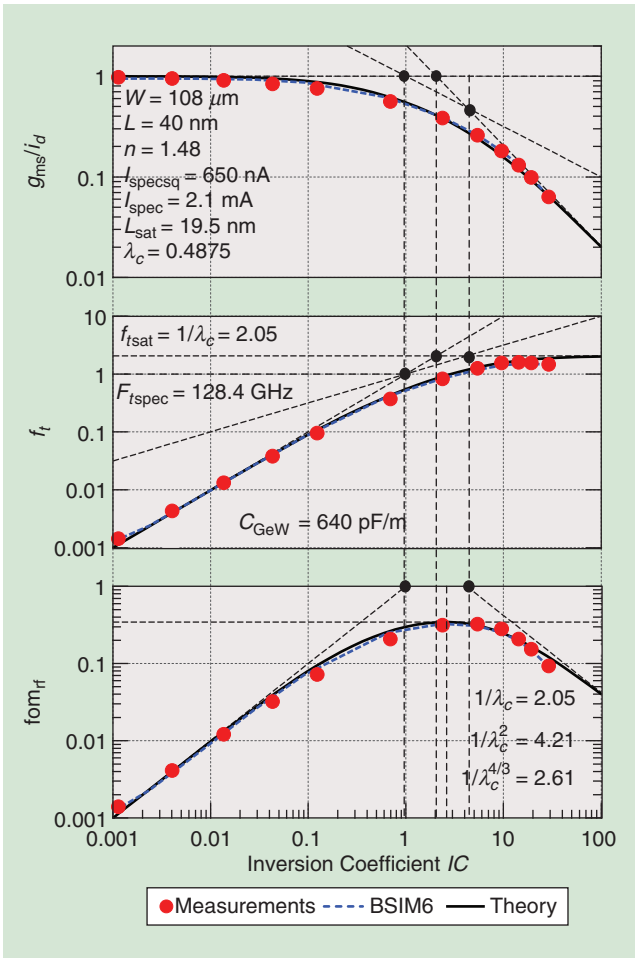

FIGURE 11: g_{ms}/i_d, f_t, and fom_{rf} versus IC for a 40-nm device [12].

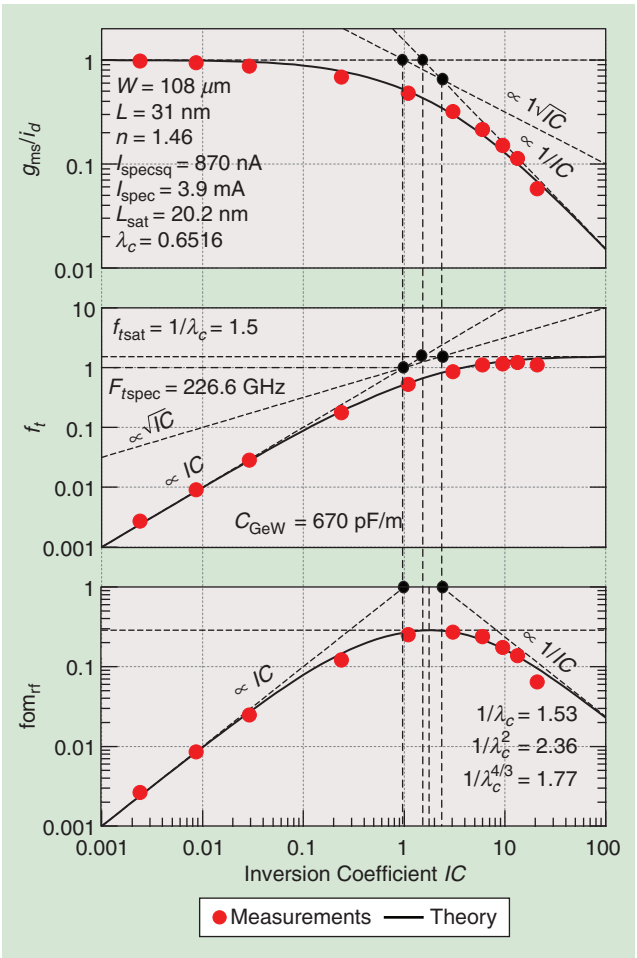

FIGURE 12: g_{ms}/i_d, f_t and fom_{rf} versus IC for a 30-nm device [12].

This article illustrates the use the IC as the main design parameter to explore the various tradeoffs faced in the design of analog circuits.

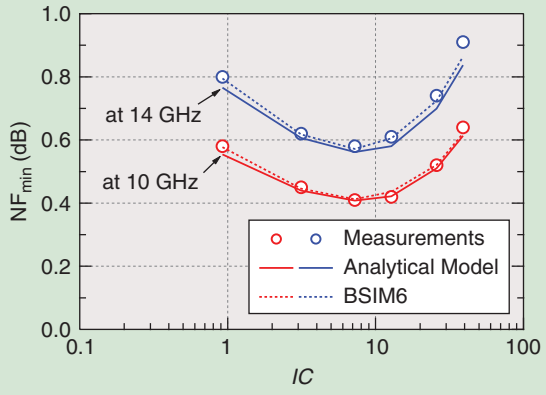

FIGURE 13: Minimum noise figure versus *IC* [11], [17].

line in Figure 10 and there would be no maximum.

Note that this FoM was successfully used by [15] to design an ultra low-power low-noise amplifier (LNA).

Experimental Results

The three FoMs presented previously are plotted versus *IC* in Figure 11 and in Figure 12 for a 40- and a 30-nm RF device from a 40- and 28-nm bulk CMOS process, respectively [12]. Despite their simplicity and reduced number of parameters, the analytical models fit the experimental data very well over almost five decades of *IC* (current). The small discrepancy for the last measurement point in SI is due to mobility reduction due to the vertical field [9], which is not accounted for in the simple model. However, this effect is accounted for in the BSIM6 compact model [16], which perfectly fits the measured data in Figure 11, including at high *IC*.

Other FoMs

Other FoMs can be defined and expressed in terms of *IC*. For example, the minimum noise figure $NF_{\min}$, which gives the minimum noise that can be achieved under proper impedance matching conditions, also shows a minimum at the higher end of MI as shown in Figure 13 [11], [17]. Another example is used for the design of low-power oscillators. An FoM including the phase noise at a given offset frequency, the power consumption, and the oscillation frequency can be defined. The latter has been evaluated for Pierce and cross-coupled oscillators and shows a maximum also at the edge of MI and WI [18], [19].

Conclusions

This article illustrates the use the *IC* as the main design parameter to explore the various tradeoffs faced in the design of analog circuits. It can help the designer to select the most appropriate *IC* setting the current and the *W*/*L* ratio. This is illustrated by looking at the simple CS gain stage. It is shown that the same transconductance, GBW, or input-referred thermal noise resistance can be achieved with lower current by shifting the *IC* toward MI at the cost of a slight increase of the transistor aspect ratio and area.

A minimum bias current can be found at an IC that lies in the middle of the MI to achieve a given GBW product when accounting for the self-loading capacitance at the drain. This current can be significantly less than the current required to achieve the same transconductance, GBW or input-referred thermal noise resistance in SI, particularly under VS. Different FoMs are then introduced, starting with the transconductance or current efficiency G_m/I_D, which tells how much transconductance is obtained for a given current. G_m/I_D is maximum in WI and decreases as $1/\sqrt{IC}$ in SI for long channel devices and as $1/(\lambda_c \cdot IC)$ for short-channel transistors because of VS. Another FoM key to evaluate the RF performance of a device is the transit frequency F_t. It is shown that F_t follows a behavior opposite of G_m/I_D, namely increasing with *IC* to reach the maximum $F_{t\text{peak}}$ in SI because of VS. It is shown that $F_{t\text{peak}}$ is simply inversely proportional to the VS parameter λ_c and that does not scale as $1/L$ but is simply proportional to the ratio of the oxide capacitance per unit area and the total extrinsic gate capacitance per unit width.

Another FoM is introduced as the product G_m/I_D and F_t that helps maximizing the *GBW*, while minimizing the added thermal noise at a given bias current, which turns out to be useful for choosing the right operating point of RF circuits such as LNAs. It is shown that the $G_m/I_D \cdot F_t$ FoM reaches a maximum in MI offering a good tradeoff between gain, noise and current consumption.

All these FoMs can be expressed versus *IC* using simple analytical expressions that fit experimental data very well despite requiring only four parameters: n, $I_{spec\square}$, L_{sat}, and C_{GeW}. All the presented FoMs are favorably compared to measurements of short-channel devices from 40- and 28-nm bulk CMOS technologies and with the BSIM6 compact model for the 40-nm

device, illustrating how powerful the concept of the IC can be.

References

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. Hoboken, NJ: McGraw-Hill, 2017.

[2] D. Binkley, *Tradeoffs and Optimization in Analog CMOS Design*, 1st ed. New York: Wiley, 2008.

[3] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET modeling: Part I," *IEEE Solid-State Circuits Mag.*, vol. 9. no. 3, pp. 26–35, Summer 2017.

[4] W. Sansen, "Minimum power in analog amplifying blocks: Presenting a design procedure," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 4, pp. 83–89, Fall 2015.

[5] C. Enz and A. Pezzotta, "Nanoscale MOSFET modeling for the design of low-power analog and RF circuits," in *Proc. Int. Conf. Mixed Design of Integrated Circuits and Systems*, June 2016, pp. 21–26.

[6] T. Melly, "Conception d'un émetteur-récepteur à faible consommation intégré en technologie CMOS," Ph.D. dissertation, EPFL, Dissertation 2231, 2000.

[7] A. Mangla, M. A. Chalkiadaki, F. Fadhuile, T. Taris, Y. Deval, and C. C. Enz, "Design methodology for ultra low-power analog circuits using next generation BSIM6 MOSFET compact model," *Microelectronics J.*, vol. 44, no. 7, pp. 570–575, July 2013.

[8] A. Mangla, "Modeling nanoscale quasi-ballistic MOS transistors," Ph.D. dissertation, EPFL, Dissertation 6385, 2014.

[9] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling—The EKV Model for Low-Power and RF IC Design*, 1st ed. Hoboken, NJ: Wiley, 2006.

[10] M. A. Chalkiadaki, "Characterization and modeling of nanoscale MOSFET for ultra-low power RF IC design," Ph.D. dissertation, EPFL, Dissertation 7030, 2016.

[11] M. A. Chalkiadaki and C. C. Enz, "RF small-signal and noise modeling including parameter extraction of nanoscale MOSFET from weak to strong inversion," *IEEE Trans. Microwave Theory Tech.*, vol. 63, no. 7, pp. 2173–2184, July 2015.

[12] C. Enz and M. A. Chalkiadaki, "Nanoscale MOSFET modeling for low-power RF design using the inversion coefficient," in *Proc. Asia-Pacific Microwave Conf.*, Dec. 2015, vol. 1, pp. 1–3.

[13] A. Shameli and P. Heydari, "Ultra-low power RFIC design using moderately inverted MOSFETs: an analytical/experimental study," in *Proc. Radio Frequency Integrated Circuits Symp.,* 2006, p. 4.

[14] A. Mangla, C. C. Enz, and J. M. Sallese, "Figure-of-merit for optimizing the current-efficiency of low-power RF circuits," in *Proc. Int. Conf. Mixed Design of Integrated Circuits and Systems*, June 2011, pp. 85–89.

[15] T. Taris, J. Begueret, and Y. Deval, "A 60μW LNA for 2.4 GHz wireless sensors network applications," in *Proc. Radio Frequency Integrated Circuits Symp.*, 2011, pp. 1–4.

[16] Y. S. Chauhan, S. Venugopalan, M. A. Chalkiadaki, M. A. U. Karim, H. Agarwal, S. Khandelwal, N. Paydavosi, J. P. Duarte, C. C. Enz, A. M. Niknejad, and C. Hu, "BSIM6: analog and RF compact model for bulk MOSFET," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 234–244, Feb. 2014.

[17] C. Enz, M. A. Chalkiadaki, and A. Mangla, "Low-power Analog/RF circuit design based on the inversion coefficient," in *Proc. European Solid-State Circuits Conf.*, Sept. 2015, pp. 202–208.

[18] F. Chicco, A. Pezzotta, and C. Enz, "Analysis of power consumption in LC oscillators based on the inversion coefficient," in *Proc. IEEE Int. Symp. Circuits and Systems Conf.*, May 2017, pp. 1514–1517.

[19] G. Guitton, A. Mangla, M. A. Chalkiadaki, F. Fadhuile, T. Taris, and C. Enz, "Design of ultra low-power RF oscillators based on the inversion coefficient methodology using BSIM6 model," *Int. J. Circuit Theory Appl.*, vol. 44, no. 2, pp. 382–397, Feb. 2016.

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