

Low-power radio design for the IoT

Exercise 8 (06.05.2021)

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Problem 1 The Common-Gate LNA

The schematic of the common-gate LNA is shown in Figure 1. Assume that the transistors are biased in saturation and that they are fabricated in a deep-submicron technology so that channel-length modulation is not negligible.

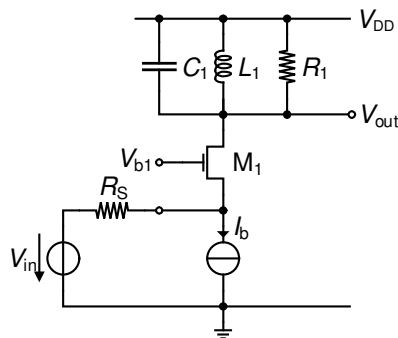


Figure 1: Common-Gate LNA

1.1 Small-signal analysis

- Draw the small-signal equivalent circuit.
- Derive the expression for the input impedance of the LNA, looking through the source of transistor M_1 , at resonance.
- Calculate the small signal gain of the circuit assuming input matching.

1.2 Noise analysis

- Draw the small-signal circuit including the noise sources.
- Calculate the noise figure of the LNA.

Problem 2 Cascode Common Gate LNA

The common-gate LNA presented in the previous problem is now cascoded with a transistor M_2 . The schematic of the cascode common-gate LNA is shown in Figure 2. Assume that the transistors are biased in saturation and that they are fabricated in a deep-submicron technology so that channel-length modulation is not negligible.

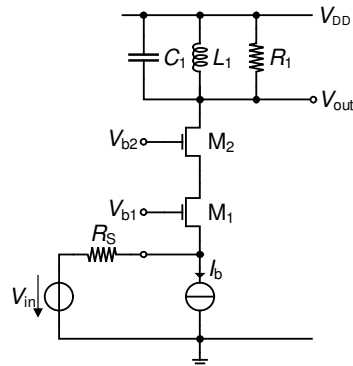


Figure 2: Cascode Common-Gate LNA

2.1 Small-signal analysis

- Draw the small-signal equivalent circuit.
- Derive the expression for the input impedance of the LNA, looking through the source of transistor M_1 , at resonance.
- Compare the input impedance with that of the common-gate LNA.
- Calculate the small signal gain of the circuit assuming input matching.

2.2 Noise analysis

- Draw the small-signal circuit including the noise sources.
- Calculate the noise contribution of transistor M_2 to the output noise (neglect the channel length modulation of M_2).
- Calculate the noise figure of the LNA.