Low-power radio design for the IoT
Exercise 8 (06.05.2021)

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Problem 1 The Common-Gate LNA

The schematic of the common-gate LNA is shown in Figure 1. Assume that the transistors are biased in saturation and that they are fabricated in a deep-submicron technology so that channel-length modulation is not negligible.

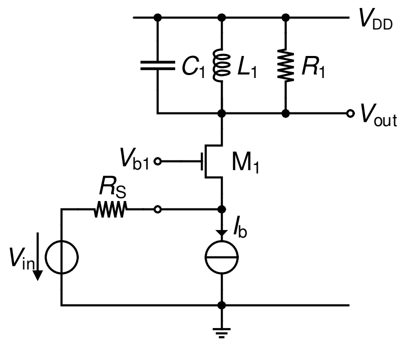

Figure 1: Common-Gate LNA

1.1 Small-signal analysis

- Draw the small-signal equivalent circuit.
- Derive the expression for the input impedance of the LNA, looking through the source of transistor M_1, at resonance.
- Calculate the small signal gain of the circuit assuming input matching.

1.2 Noise analysis

- Draw the small-signal circuit including the noise sources.
- Calculate the noise figure of the LNA.

Problem 2 Cascode Common Gate LNA

The common-gate LNA presented in the previous problem is now cascoded with a transistor M_2. The schematic of the cascode common-gate LNA is shown in Figure 2. Assume that the transistors are biased in saturation and that they are fabricated in a deep-submicron technology so that channel-length modulation is not negligible.

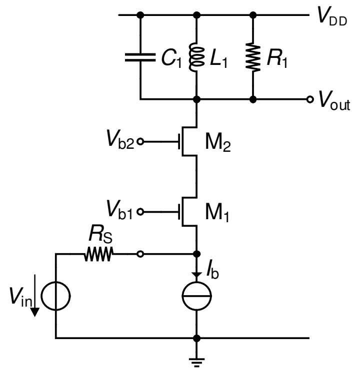

Figure 2: Cascode Common-Gate LNA

2.1 Small-signal analysis

- Draw the small-signal equivalent circuit.
- Derive the expression for the input impedance of the LNA, looking through the source of transistor M_1, at resonance.
- Compare the input impedance with that of the common-gate LNA.
- Calculate the small signal gain of the circuit assuming input matching.

2.2 Noise analysis

- Draw the small-signal circuit including the noise sources.
- Calculate the noise contribution of transistor M_2 to the output noise (neglect the channel length modulation of M_2).
- Calculate the noise figure of the LNA.

Solutions to Exercise 8 (06.05.2021)

Problem 1 Analysis of Common-Gate LNA

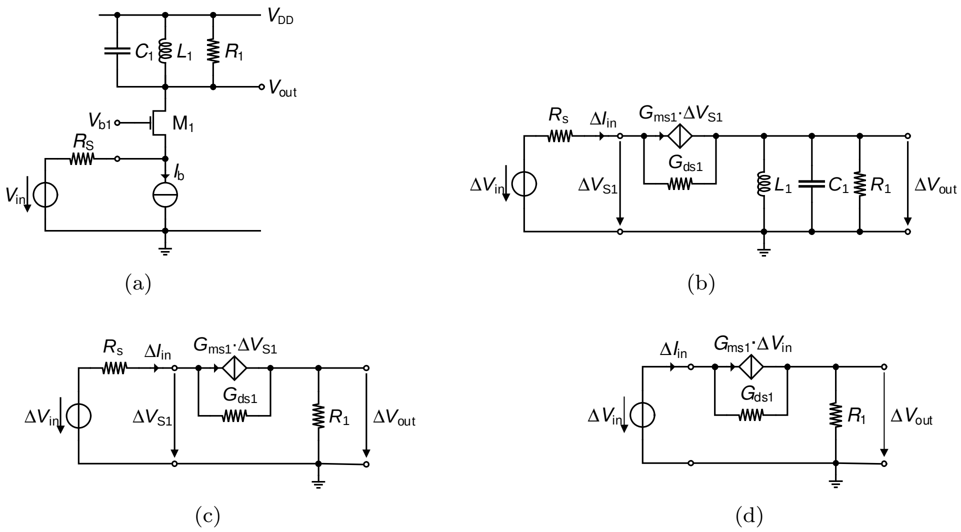

Figure 1: a) Schematic of the common-gate LNA. b) Corresponding small-signal schematic. c) Corresponding small-signal schematic at resonance. d) Small-signal schematic used for input impedance calculation.

1.1 Small Signal Analysis

- Draw the small-signal equivalent circuit.
- Derive the expression for the input impedance of the LNA, looking through the source of transistor M_1, at resonance.
- Calculate the small signal gain of the circuit assuming input matching.

Fig. 1(b) shows the small-signal schematic of the common-gate LNA. At resonance, the small-signal schematic reduces to that of Fig. 1(c). The input impedance of the circuit looking through the source of M_1, can then be calculated as

$$Z_{in} \triangleq \left.\frac{\Delta V_{in}}{\Delta I_{in}}\right|_{I_{out}=0} = \frac{1 + R_1 G_{ds1}}{G_{ms1} + G_{ds1}}. \tag{1}$$

Assuming that the intrinsic gain of M_1, G_{ms1}/G_{ds1}, is much greater than unity, (1) reduces to

$$Z_{in} \cong \frac{1}{G_{ms1}} + \frac{R_1}{G_{ms1}/G_{ds1}}. \tag{2}$$

Eq. (2) reveals the impact of the drain conductance on input impedance of the LNA. In modern technologies the intrinsic gain G_{ms1}/G_{ds1} is quite low (of the order of 10). Thus, the second term in (2) could be comparable to or even exceed the $1/G_{ms1}$ term, resulting in an increase of the input impedance and making it difficult to match to a 50 Ω resistance.

The small-signal gain can be calculated from the schematic in Fig. 1(c) resulting in

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{R_1(G_{ms1} + G_{ds1})}{1 + R_1 G_{ds1} + R_S(G_{ms1} + G_{ds1})} = \frac{G_{ms1} R_1 (1 + G_{ds1}/G_{ms1})}{1 + R_1 G_{ds1} + G_{ms1} R_S (1 + G_{ds1}/G_{ms1}))}. \tag{3}$$

For a long-channel device, we can assume that $G_{ms1} \gg G_{ds1}$. If additionally it is assumed that $G_{ms1} R_S \ll 1$ and $R_1 G_{ds1} \ll 1$, then (3) reduces to

$$A_v \cong G_{ms1} \cdot R_1. \tag{4}$$

For matched input, i.e., $Z_{in} = R_S$, using (1) in (3), we obtain,

$$A_v\big|_{matched} = \frac{R_1(G_{ms1} + G_{ds1})}{2(1 + R_1 G_{ds1})}. \tag{5}$$

If R_1 is comparable to $1/G_{ds1}$, then the voltage gain of the common-gate LNA stage is of the order of $G_{ms1}/4G_{ds1}$, which is a very low value compared to the value obtained for a long-channel device

$$A_v\big|_{matched} = \frac{G_{ms1} R_1}{2}. \tag{6}$$

1.2 Noise analysis

- Draw the small-signal circuit including the noise sources.
- Calculate the noise figure of the LNA.

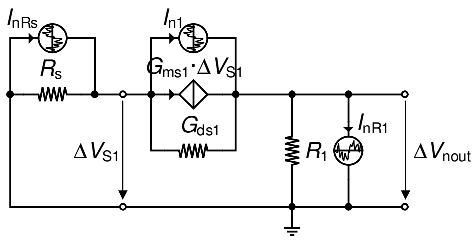

Figure 2: Small signal schematic showing the noise sources.

The output noise voltage can be calculated from the small-signal schematic including all the noise sources shown in Fig. 2 as

$$V_{nout} = R_{mRs} \cdot I_{nRs} + R_{m1} \cdot I_{n1} + R_{mR1} \cdot I_{nR1}, \tag{7}$$

with

$$R_{mRs} = A_v \cdot R_S, \tag{8a}$$

$$R_{m1} = \frac{R_1}{1 + (G_{ms1} + G_{ds1})R_S + G_{ds1} R_1}, \tag{8b}$$

$$R_{mR1} = -\frac{R_1(1 + (G_{ms1} + G_{ds1})R_S)}{1 + (G_{ms1} + G_{ds1})R_S + G_{ds1} R_1}. \tag{8c}$$

The output thermal noise resistance is then equal to

$$R_{nout} = |R_{mRs}|^2 \cdot \frac{1}{R_S} + |R_{m1}|^2 \cdot G_{n1} + |R_{mR1}|^2 \cdot \frac{1}{R_1}, \tag{9}$$

where $G_{n1} = \delta_{nD1} \cdot G_{ms1}$. The input thermal noise resistance is then given by dividing (9) by $|A_v|^2$, resulting in

$$R_{nin} = R_S + \frac{\delta_{nD1} \cdot G_{ms1}}{(G_{ms1} + G_{ds1})^2} + \left(\frac{1 + (G_{ms1} + G_{ds1})R_S}{(G_{ms1} + G_{ds1})R_S}\right)^2 \cdot \frac{R_S^2}{R_1}. \tag{10}$$

For a long-channel device $G_{ms1} \gg G_{ds1}$ and (10) reduces to

$$R_{nin} \cong R_S + \frac{\delta_{nD1}}{G_{ms1}} + \left(1 + \frac{1}{G_{ms1} R_S}\right)^2 \cdot \frac{R_S^2}{R_1}. \tag{11}$$

The noise factor is then given by

$$F = \frac{R_{nin}}{R_S} = 1 + \frac{\delta_{nD1} \cdot G_{ms1}}{R_S (G_{ms1} + G_{ds1})^2} + \left(\frac{1 + (G_{ms1} + G_{ds1})R_S}{(G_{ms1} + G_{ds1})R_S}\right)^2 \cdot \frac{R_S}{R_1}, \tag{12}$$

which for a long-channel device reduces to

$$F \cong 1 + \frac{\delta_{nD1}}{G_{ms1} R_S} + \left(1 + \frac{1}{G_{ms1} R_S}\right)^2 \cdot \frac{R_S}{R_1}. \tag{13}$$

Under impedance matching $G_{ms1} R_S = 1$ and (13) reduces to

$$F\Big|_{matched} \cong 1 + \delta_{nD1} + 4\frac{R_S}{R_1}. \tag{14}$$

Problem 2 Analysis of the Cascode Common-Gate LNA

2.1 Small Signal Analysis

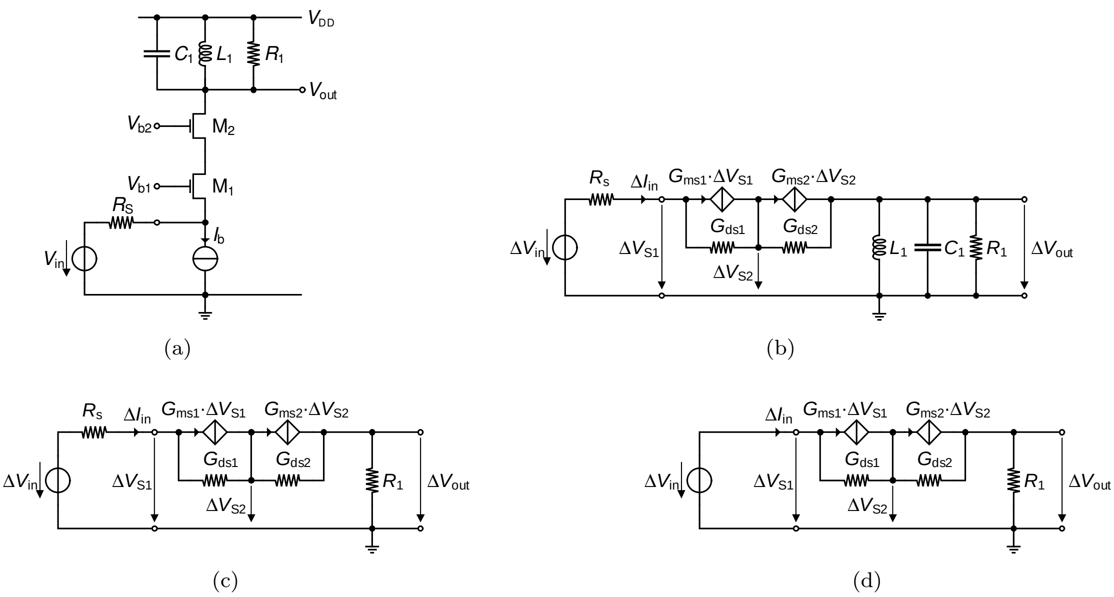

Figure 3: a) Schematic of the common-gate LNA. b) Corresponding small-signal schematic. c) Corresponding small-signal schematic at resonance. d) Small-signal schematic used for input impedance calculation.

2.2 Small-signal analysis

- Draw the small-signal equivalent circuit.
- Derive the expression for the input impedance of the LNA, looking through the source of transistor M_1, at resonance.
- Compare the input impedance with that of the common-gate LNA.
- Calculate the small signal gain of the circuit assuming input matching.

The problem of high input impedance of the common-gate LNA can be alleviated by introducing a cascode transistor as shown in Fig. 3(a). Its small-signal schematic is shown in Fig. 3(b) which at resonance reduces to Fig. 3(c).

The input impedance of the circuit looking through the source of M_1 can easily be calculated from the schematic shown in Fig. 1(d) resulting in

$$Z_{in} \triangleq \frac{\Delta V_{in}}{\Delta I_{in}}\bigg|_{\Delta I_{out}=0} = \frac{G_{ds1} + G_{ds2} + G_{ms2} + G_{ds1} G_{ds2} R_1}{(G_{ds1} + G_{ms1})(G_{ds2} + G_{ms2})}. \tag{15}$$

Assuming that the intrinsic gain of M_1 and M_2 are much greater than unity, i.e. $G_{ms1}/G_{ds1} \gg 1$ and $G_{ms2}/G_{ds2} \gg 1$ results in

$$Z_{in} \cong \frac{1}{G_{ms1}} + \frac{G_{ds1}G_{ds2}R_1}{G_{ms1} \cdot G_{ms2}} \tag{16}$$

The second term in (16) shows that R_1 is divided by the intrinsic gains of two transistors and therefore its effect on input impedance is negligible (compare with (2)). Hence,

$$Z_{in} \cong \frac{1}{G_{ms1}}. \tag{17}$$

The voltage gain assuming again that $G_{ms1}/G_{ds1} \gg 1$ and $G_{ms2}/G_{ds2} \gg 1$ is then given by

$$A_v \cong \frac{G_{ms1}R_1}{1 + G_{ms1}R_S}, \tag{18}$$

which turns out to be independent of G_{ms2}. The small-signal voltage assuming input matching $Z_{in} = 1/G_{ms1} = R_S$ reduces to

$$A_v \cong \frac{G_{ms1}R_1}{2}. \tag{19}$$

2.3 Noise analysis

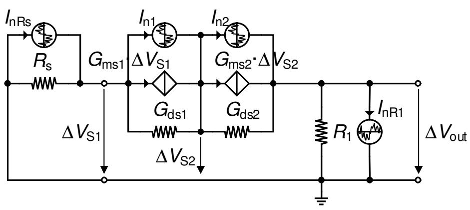

Figure 4: Small signal schematic showing the noise sources.

- Draw the small-signal circuit including the noise sources.
- Calculate the noise contribution of transistor M_2 to the output noise (neglect the channel length modulation of M_2).
- Calculate the noise figure of the LNA.

The derivation of the output noise voltage can be simplified by neglecting G_{ds2} in the schematic of Fig. 4. Note that if we also neglect G_{ds1}, then the noise coming from M_2 is zero. After solving the Kirkhoff equations and assuming that $G_{ms1}/G_{ds1} \gg 1$ and $G_{ds1}R_S \ll 1$, we get the output noise voltage as

$$V_{nout} \cong \frac{R_1}{1 + G_{ms1}R_S} \cdot I_{n1} + \frac{G_{ds1}R_1}{G_{ms2}(1 + G_{ms1}R_S)} \cdot I_{n2} - R_1 \cdot I_{nR1} + \frac{G_{ms1}R_1R_S}{1 + G_{ms1}R_S} \cdot I_{nRs} \tag{20}$$

The corresponding output noise resistance is then given by

$$R_{nout} \cong \left(\frac{R_1}{1 + G_{ms1}R_S}\right)^2 \cdot G_{n1} + \left(\frac{G_{ds1}R_1}{G_{ms2}(1 + G_{ms1}R_S)}\right)^2 \cdot G_{n2} + R_1^2 \cdot G_1 + \left(\frac{G_{ms1}R_SR_1}{1 + G_{ms1}R_S}\right)^2 \cdot G_S, \tag{21}$$

where $G_S \triangleq 1/R_S$, $G_1 \triangleq 1/R_1$. The input-referred noise resistance is given by dividing (21) by the square of the voltage gain (18), resulting in

$$R_{nin} \cong R_S + \frac{G_{n1}}{G_{ms1}^2} + \left(\frac{G_{ds1}}{G_{ms1}G_{ms2}}\right)^2 \cdot G_{n2} + \left(\frac{1 + G_{ms1}R_S}{G_{ms1}}\right)^2 \frac{1}{R_1} \tag{22}$$

$$\cong R_S + \frac{G_{n1}}{G_{ms1}^2} + \left(\frac{1 + G_{ms1}R_S}{G_{ms1}}\right)^2 \frac{1}{R_1}. \tag{23}$$

From (24), we see that, like in a normal cascode, the noise contribution from M_2 is divided by the square of the intrinsic gain of the driver transistor M1 and can hence be neglected. This is without accounting for the parasitic capacitance at the cascode node which lowers the gain and increases the contribution of M2 to the input-referred noise. At RF we are mostly interested by the thermal noise coming from M_1 and M_2. Hence we can replace G_{n1} and G_{n2} by $\delta_{nD1} \cdot G_{ms1}$ and $\delta_{nD2} \cdot G_{ms2}$, resulting in

$$R_{nin} \cong R_S + \frac{\delta_{nD1}}{G_{ms1}} + \frac{\delta_{nD2} G_{ds1}^2}{G_{ms1}^2 G_{ms2}} + \left(\frac{1 + G_{ms1} R_S}{G_{ms1}}\right)^2 \frac{1}{R_1} \tag{24}$$

$$\cong R_S + \frac{\delta_{nD1}}{G_{ms1}} + \left(\frac{1 + G_{ms1} R_S}{G_{ms1}}\right)^2 \frac{1}{R_1}. \tag{25}$$

The corresponding noise factor is then given by

$$F \triangleq \frac{R_{nin}}{R_S} \cong 1 + \frac{\delta_{nD1}}{G_{ms1} R_S} + \frac{\delta_{nD2} G_{ds1}^2}{G_{ms1}^2 G_{ms2} R_S} + \frac{(1 + G_{ms1} R_S)^2}{G_{ms1}^2 R_S R_1} \tag{26}$$

$$\cong 1 + \frac{\delta_{nD1}}{G_{ms1} R_S} + \frac{(1 + G_{ms1} R_S)^2}{G_{ms1}^2 R_S R_1}. \tag{27}$$

Under matched condition $Z_{in} = 1/G_{ms1} = R_S$ we have

$$F\big|_{matched} \cong 1 + \delta_{nD1} + \frac{\delta_{nD2} G_{ds1}^2}{G_{ms1} G_{ms2}} + \frac{4}{G_{ms1} R_1}. \tag{28}$$