MICRO-461
Low-power Radio Design for the IoT

5. Modeling of active and passive devices at RF

Passive Devices

Christian Enz

Integrated Circuits Lab (ICLAB), Institute of Microengineering (IMT), School of Engineering (STI)

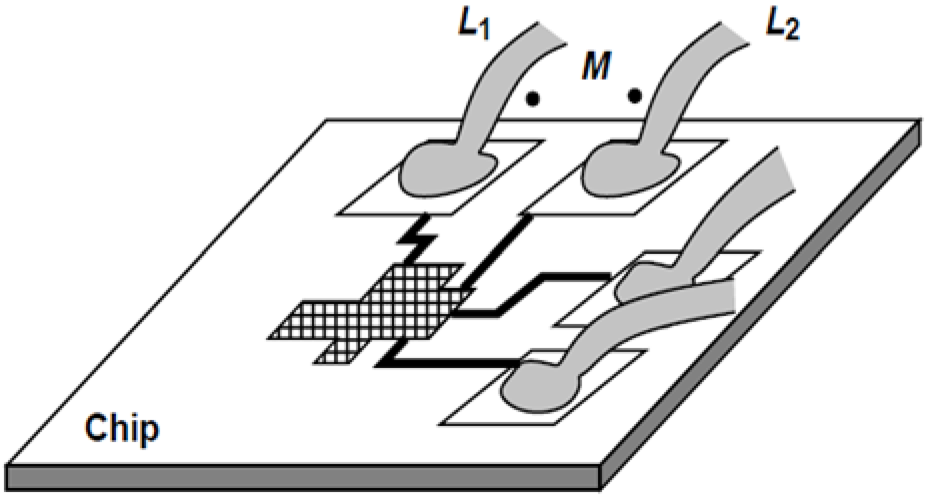
Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland

EPFL

Outline

- **Introduction**
- Inductors
- Transformers
- Varactors

Introduction

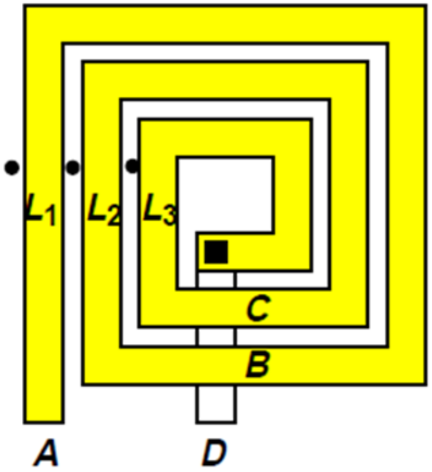


- Reduction of off-chip components translates into a reduction of system cost
- Modeling issues of off-chip inductors
- The bond wires and package pins connecting chip to outside world may experience significant coupling

Outline

- Introduction
- **Inductors**
- Transformers
- Varactors

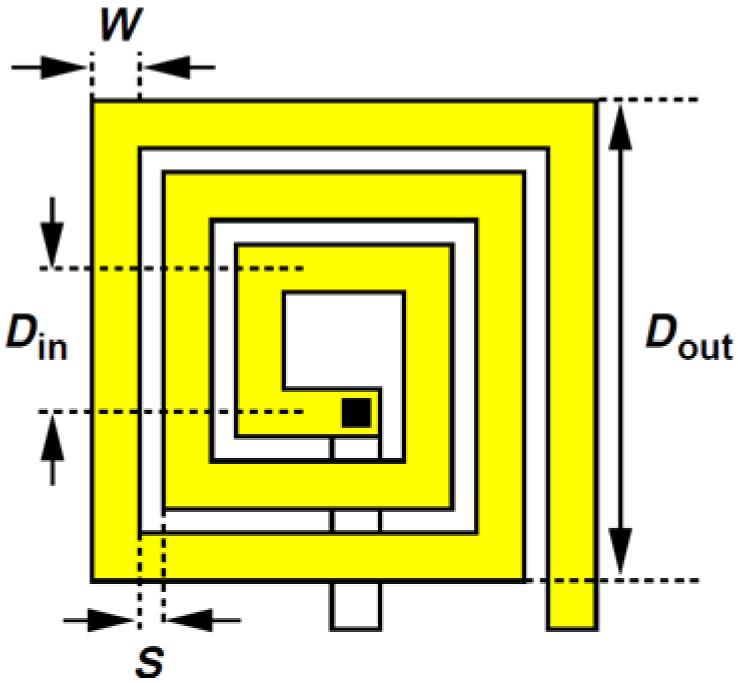
Basic Planar Inductor Structure



$$L_{tot} = L_1 + L_2 + L_3 + M_{12} + M_{13} + M_{23}$$

- Has mutual coupling between every two turns and larger inductance than straight wire
- Spiral is implemented on top metal layer to minimize parasitic resistance and capacitance
- Inductance of an N-turn planar spiral structure inductor has $N(N+1)/2$ terms
- Factors that limit the growth rate of an inductance of spiral inductor as function of N:
  - Due to planar geometry the inner turns have smaller size and exhibit smaller inductance.
  - The mutual coupling factor is about 0.7 for adjacent turns hence contributing to lower inductance.

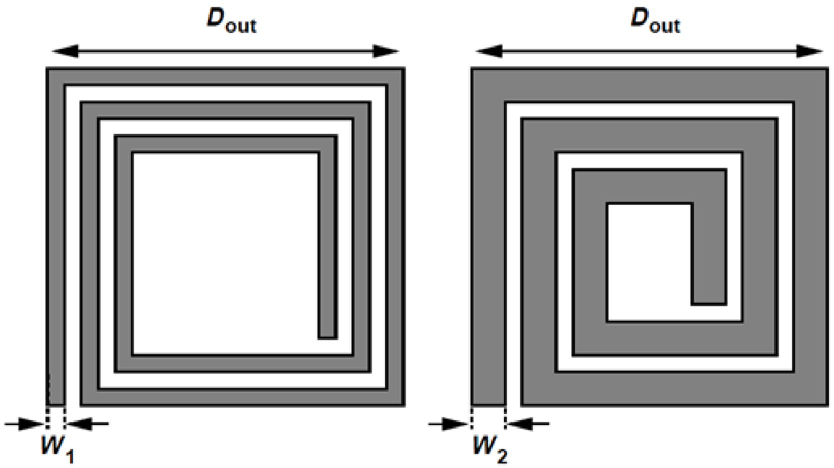
Geometry of Inductor Effects Inductance



Various dimensions of a spiral inductor

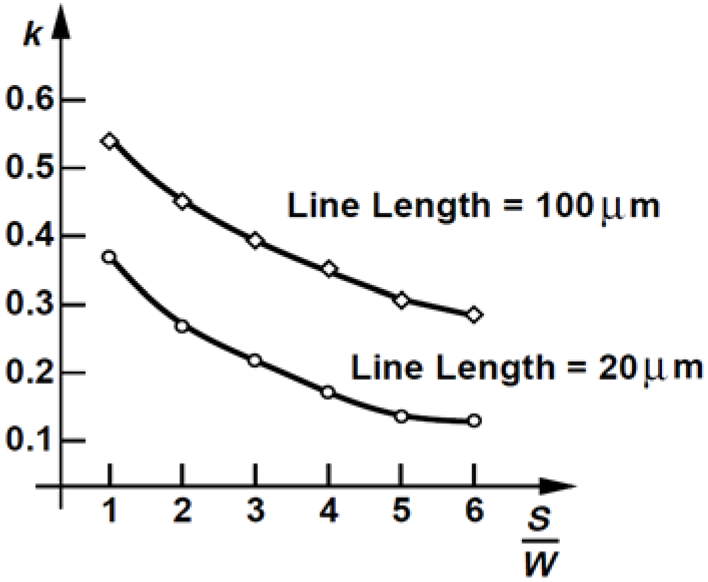
- A two dimensional square spiral inductor is fully specified by following four quantities:
  - Outer dimension, D_{out}
  - Line width, W
  - Line spacing, S
  - Number of turns, N

Effect of Doubling Line Width of Inductor



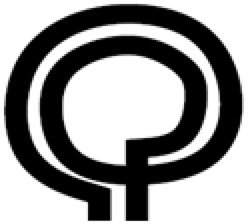
- Doubling the width inevitably decreases the diameter of inner turn, thus lowering their inductance
- The spacing between the legs reduces, hence their mutual inductance also decrease

Magnetic Coupling Factor Plot

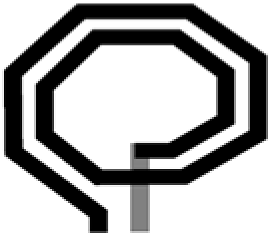


- Coupling factor between 2 straight metal lines as a function of their normalized spacing S/W
- Obtained from electromagnetic field simulations

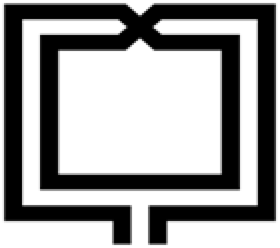
Inductor Structures Encountered in RFIC Design



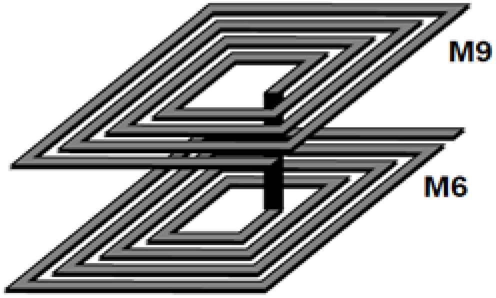
Circular



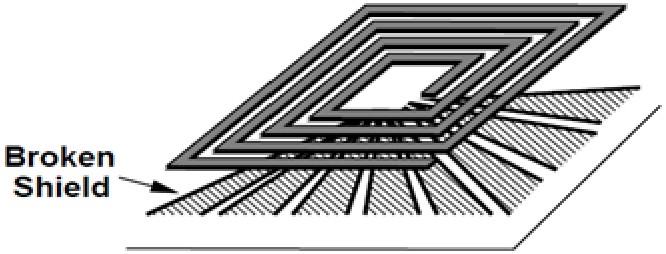
Octagonal



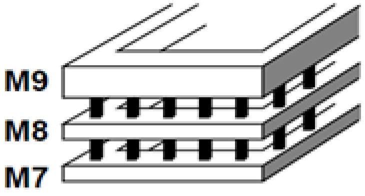
Symmetric



Stacked



With Grounded shield



Parallel Spirals

- Various inductor geometries shown above are result of improving the trade-offs in inductor design, specifically those between:
    - The quality factor and the capacitance
    - The inductance and the dimensions
- Note that these various inductor geometries provide additional degrees of freedom but also complicate the modeling task

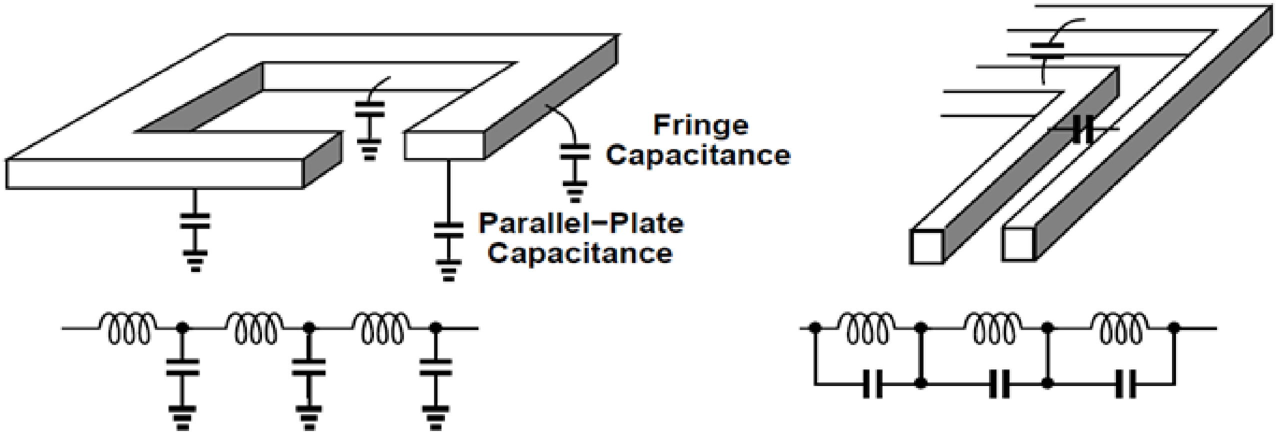
Inductance Equations

- Closed form inductance equations can be found based on
  - Curve fitting methods
  - Physical properties of inductors
- Various expressions have been reported in literature [1,2,3]. For example, an empirical formula that has less than 10% error for inductors in the range of 5 to 50 nH is given in [1] and can be reduced to the following form for a square spiral

$$L \approx 1.3 \times 10^{-7} \frac{A_m^{5/3}}{A_{tot}^{1/6} W^{1.75} (W+S)^{0.25}},$$

- Where A_m is the metal area (the shaded area) and $A_{tot} \cong D_{out}^2$ is the total inductor area
- All units are metric

Parasitic Capacitance of Integrated Inductors

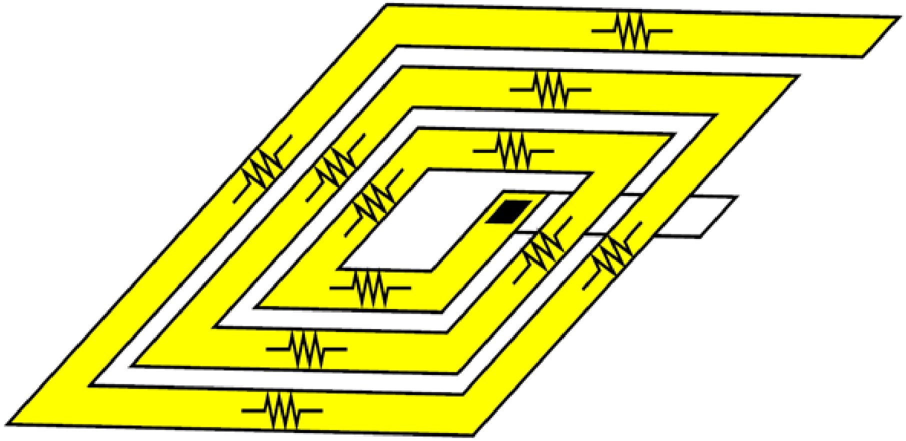


(a)

(b)

- Planar spiral inductor suffers from parasitic capacitance because the metal lines of the inductor exhibit parallel plate capacitance and adjacent turns bear fring capacitance

Loss Mechanisms: Metal Resistance



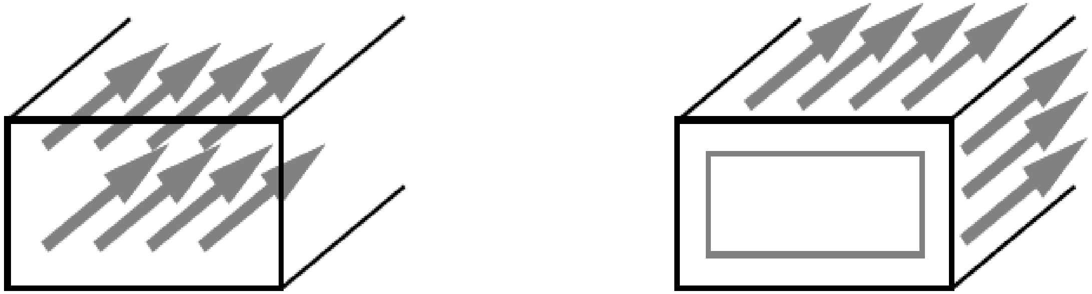
- Suppose the metal line forming an inductor exhibits a series resistance, R_S
- The Q may be defined as the ratio of the desirable impedance, $\omega_0 L_1$, and the undesirable impedance, R_S:

$$Q = \frac{L_1 \omega_0}{R_S}$$

- For example, a 5-nH inductor operating at 5 GHz with an R_S of 15.7Ω has a Q of 10

Loss Mechanisms – Skin Effect

Current distribution in a conductor



(a) At low frequency (b) At high frequency

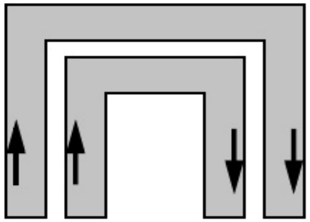
- The skin depth δ is given by

$$\delta = \frac{1}{\sqrt{\pi \cdot f \cdot \mu \cdot \sigma}}$$

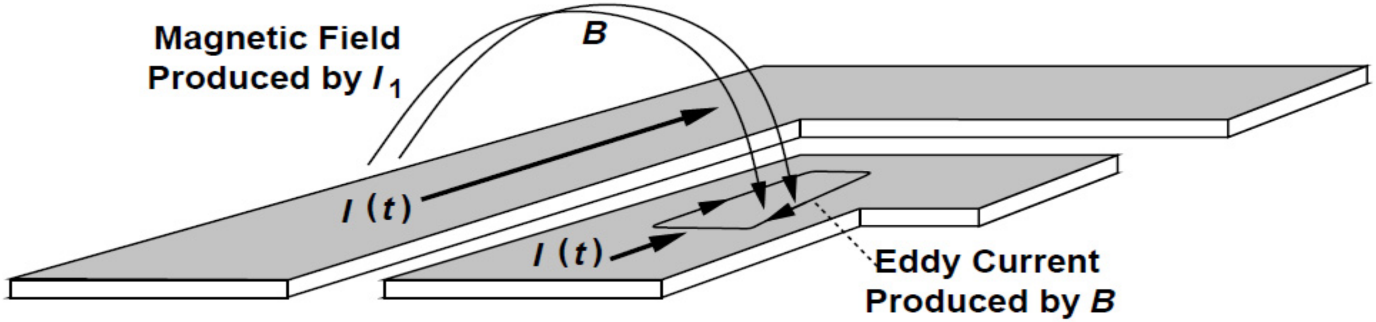
- where f denotes the frequency, μ the permeability, and σ the conductivity. For example, δ ≈ 1.4µm at 10 GHz for aluminum. The extra resistance of a conductor due to the skin effect is equal to

$$R_{skin} = \frac{1}{\sigma \cdot \delta}$$

Skin Effect – Current Crowding Effect



(a) Current distribution in adjacent turns



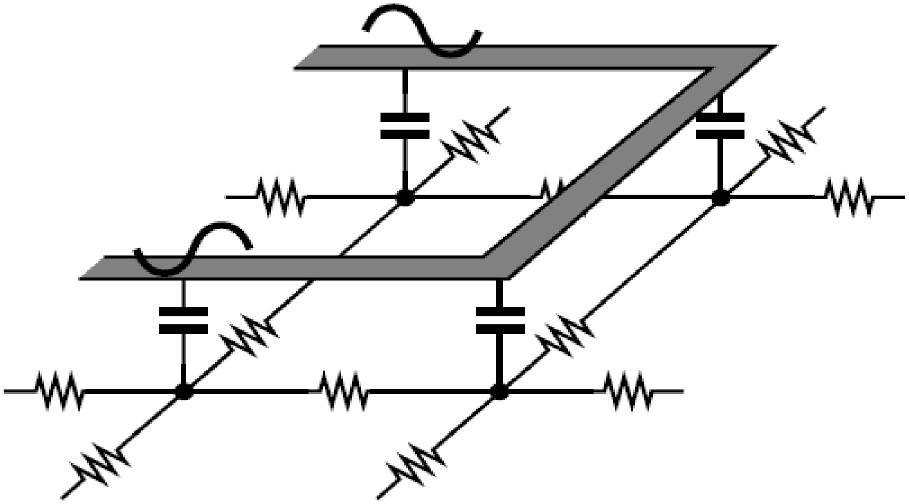
(b) Detailed view of (a)

- For $f \geq f_{crit}$, the magnetic field produced by adjacent turn induces eddy current, causing unequal distribution of current across the conductor width, hence altering the effective resistance of the turn
- For $f \geq f_{crit}$, the effective resistance R_{eff} therefore increases according to

$$R_{eff} \cong R_0 \left[1 + \frac{1}{10} \left(\frac{f}{f_{crit}} \right)^2 \right] \quad \text{with} \quad f_{crit} \cong \frac{3.1}{2\pi\mu} \frac{W+S}{W^2} R_{\square}$$

- Where $R_{\square}$ represents the dc sheet resistance of the metal

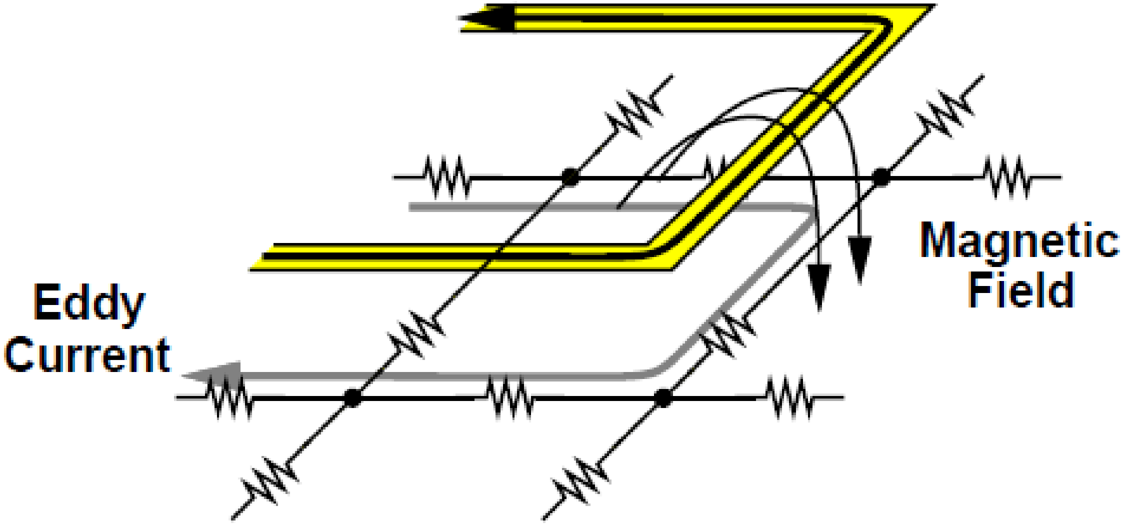
Capacitive Coupling to Substrate



Substrate loss due to capacitive coupling

- Voltage at each point of the spiral rise and fall with time causing displacement current flow between this capacitance and substrate
- This current causes loss and reduces the Q of the inductor

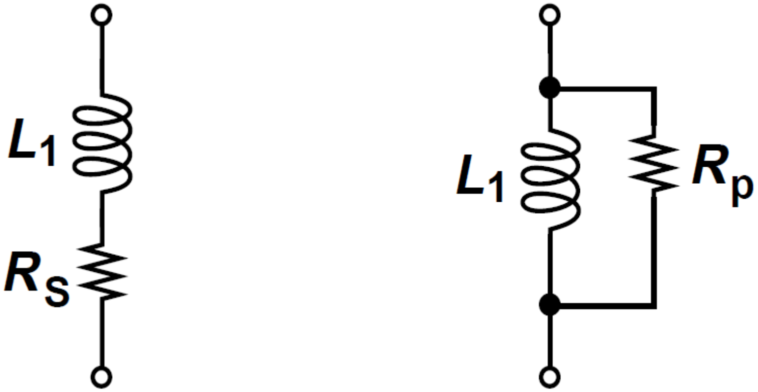
Magnetic Coupling to Substrate



- The time varying inductor current generates eddy current in the substrate
- Lenz's law states that this current flows in the opposite direction
- The induction of eddy currents in the substrate can be viewed as transformer coupling

Modeling Loss by Series or Parallel Resistor

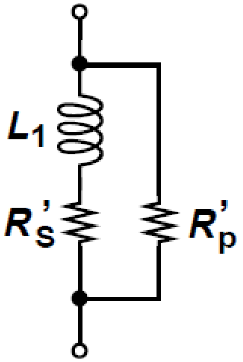
$$Q = \frac{\omega L_1}{R_S}$$



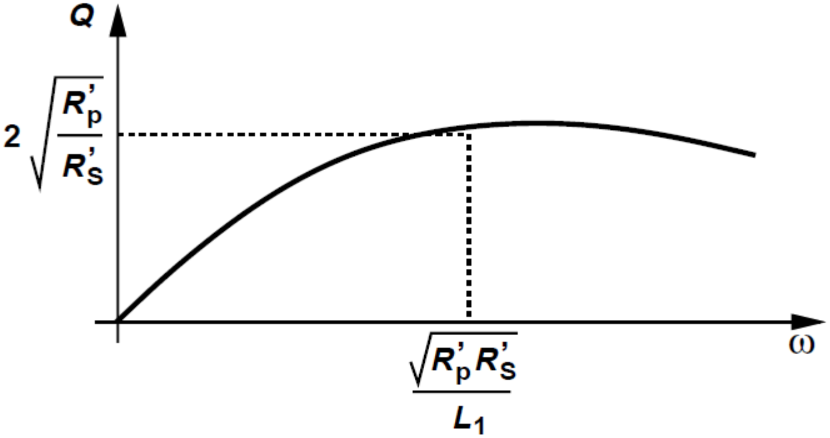
$$Q = \frac{R_p}{\omega L_1}$$

- A constant series resistance R_S model inductor loss for limited range of frequencies
- A constant parallel resistance R_p model inductor loss for narrow range of frequencies
- Note that the behavior of Q of inductor predicted by above two models has suggested opposite trends of Q with frequency

Modeling Loss by Both Series and Parallel Resistors



Modeling loss by both parallel and series resistances



Resulting behavior of Q

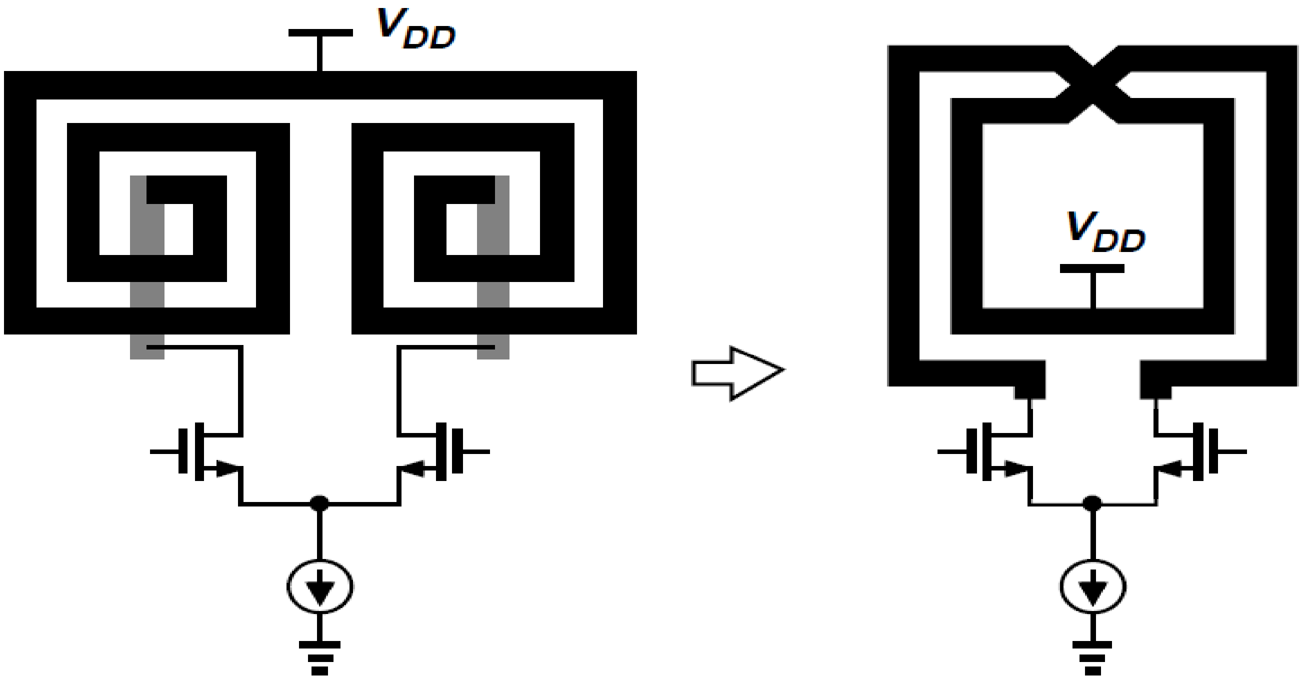
$$R'_S = \frac{\omega L_1}{2Q} \quad \text{and} \quad R'_p = 2Q\omega L_1$$

- The overall Q of the inductor is then given by

$$Q = \frac{\omega R'_p L_1}{\omega^2 L_1^2 + R'_S \cdot \left(R'_S + R'_p\right)}$$

- Which shows a maximum at $\sqrt{R'_p R'_S / L_1}$

Symmetric Inductor



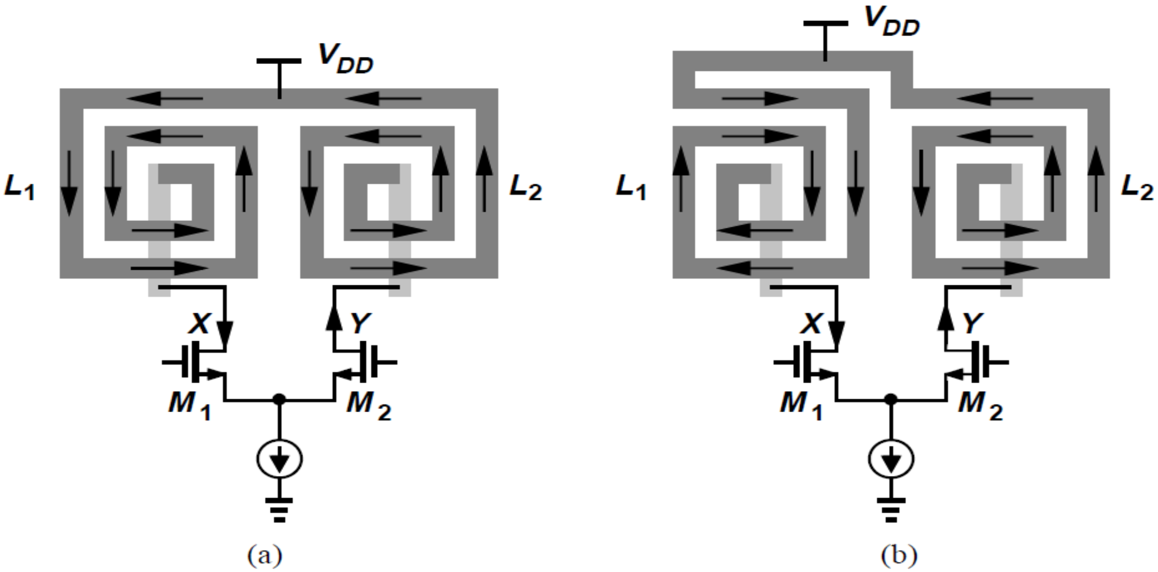
- Differential circuits can employ a single symmetric inductor instead of two asymmetric inductors
- It has two advantages:
  - Save area
  - Differential geometry also exhibit higher Q

Mirror/Step Symmetry of Single Ended Inductor

Load inductors in a differential pair

Mirror symmetry

Step symmetry



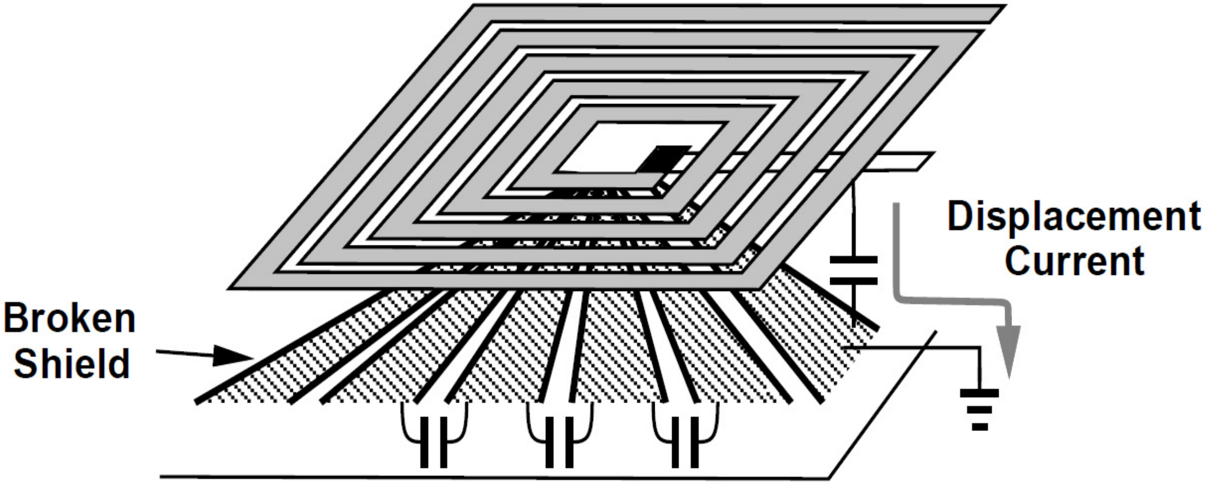
$$L_{eq} = L_1 + L_2 - 2M$$

$$L_{eq} = L_1 + L_2 + 2M$$

- Lower Q

- Higher Q

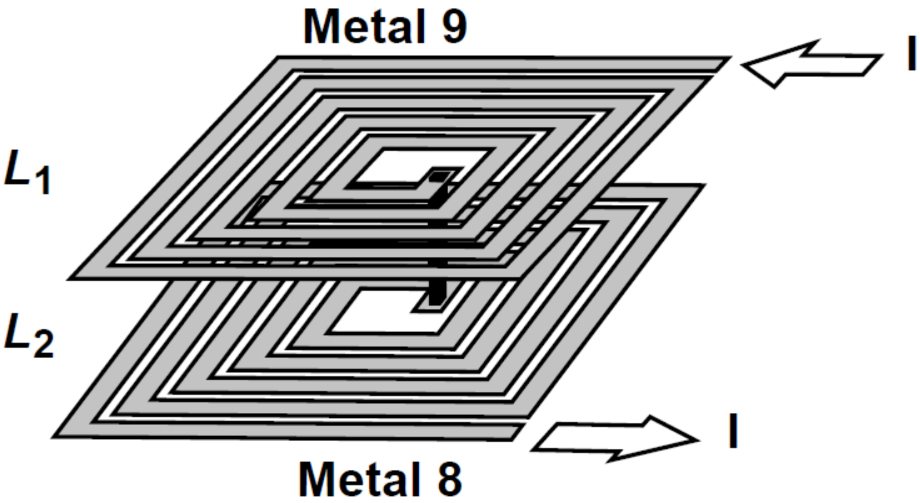
Inductors with Ground Shield



- This structure allows the displacement current to flow through the low resistance path to ground to avoid electrical loss through substrate
- Eddy currents through a continuous shield drastically reduce inductance and Q, so a “patterned” shield is used
- This shield reduces the effect of capacitive coupling to substrate
- Eddy currents of magnetic coupling still flows through substrate

Stacked Inductors

$$L_{tot} = L_1 + L_2 + 2M$$
$$M = L_1 = L_2$$
$$L_{tot} = 4L$$



- Similarly, N stacked spiral inductor operating in series raises total inductance by a factor of N_2

Outline

- Introduction
- Inductors
- **Transformers**
- Varactors

Transformers

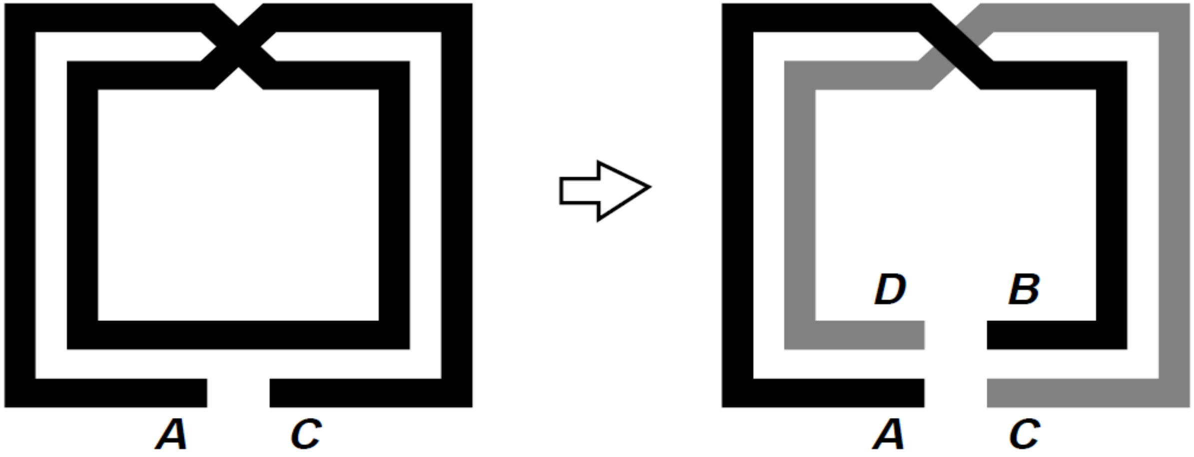
Useful function of transformer in RF Design:

- Impedance matching
- Feedback and feedforward with positive and negative polarity
- Single ended to differential conversion and vice-verse.
- AC coupling between stages

Characteristics of Well-designed Transformers

- Low series resistance in primary and secondary windings
- High magnetic coupling between primary and secondary windings
- Low capacitive coupling between primary and secondary windings
- Low parasitic capacitance to the substrate

Transformer Structures

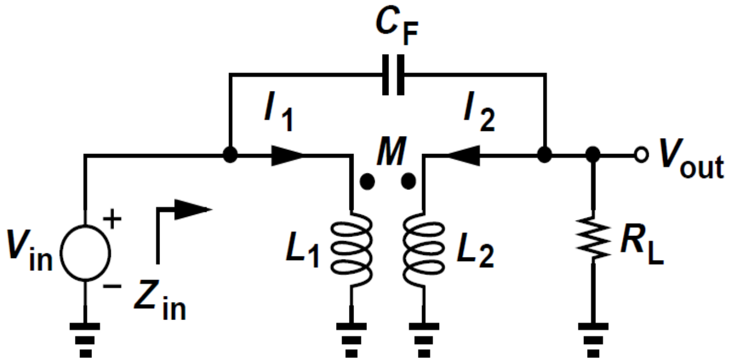


Transformer derived from a symmetric inductor

$$L_{AC} = 2L_{AB} + 2M$$

- Segments AB and CD are mutually coupled inductors
- Primary and secondary are identical so this is 1:1 transformer

Simple Transformer Model and its Transfer Function



- The transformer action gives

$$V_{in} = sL_1 \cdot I_1 + sM \cdot I_2$$

$$V_{out} = sM \cdot I_1 + sL_2 \cdot I_2$$

- Finding I_1 from 1st equation and replacing in the 2nd equation leads to

$$I_2 = \frac{V_{out}}{sL_2} - \frac{M\left(V_{in} - sM \cdot I_2\right)}{sL_1 L_2}$$

- KCL at output node yields

$$sC_F \cdot \left(V_{in} - V_{out}\right) - I_2 = \frac{V_{out}}{R_L}$$

Simple Transformer Model and its Transfer Function

- Replacing I_2 in above equation and simplifying the result, we obtain

$$\frac{V_{out}}{V_{in}} = \frac{s^2 L_1 L_2 C_F \cdot \left(1 - \frac{M^2}{L_1 L_2}\right) + M}{s^2 L_1 L_2 C_F \cdot \left(1 - \frac{M^2}{L_1 L_2}\right) + s \frac{L_1 L_2}{R_L} \cdot \left(1 - \frac{M^2}{L_1 L_2}\right) + L_1}$$

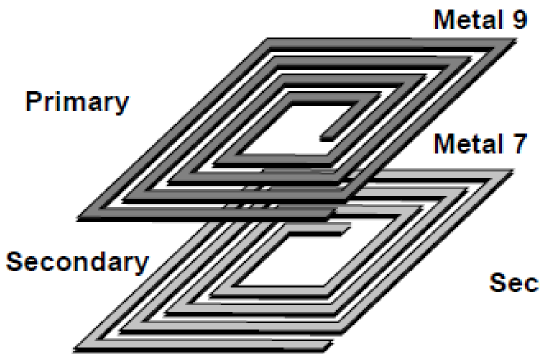
- Setting $C_F = 0$ in the above equation leads to the input to output transfer function

$$\frac{V_{out}}{V_{in}} = \frac{M}{s \frac{L_1 L_2}{R_L} \cdot \left(1 - \frac{M^2}{L_1 L_2}\right) + L_1}$$

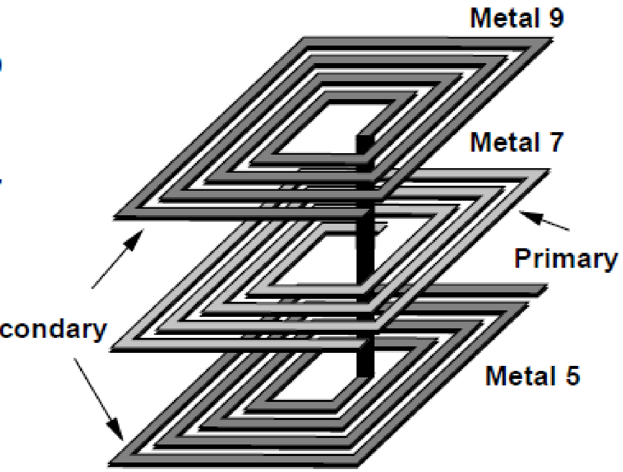
- The input impedance is given by

$$Z_{in} = sL_1 - \frac{s^2 M^2}{R_L + sL_2}$$

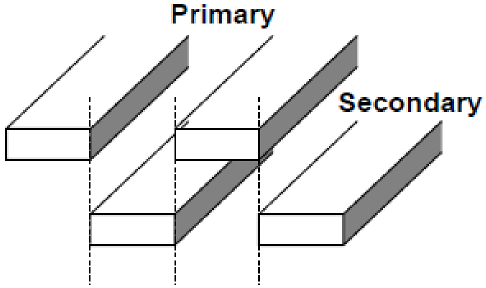
Stacked Transformers



One to one Stack transformer



One to two Stack transformer



Staggering of turns to reduce capacitive coupling

- Higher magnetic coupling
- Unlike planar structures, primary and secondary can be identical and symmetrical
- Overall area is less than planar structure
- Larger capacitive coupling compared to planar structure

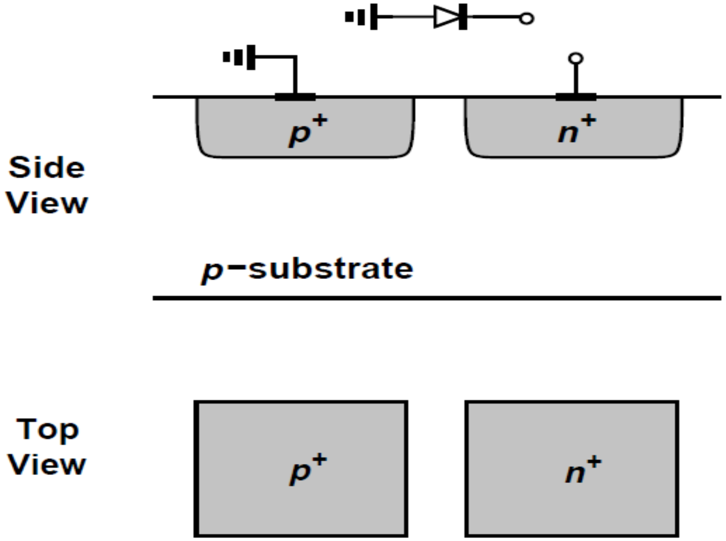
Outline

- Introduction
- Inductors
- Transformers
- **Varactors**

Varactors

- Varactor is a voltage-dependent capacitor
- Two important attributes of varactor design become critical in oscillator design
  - The capacitance range i.e. ratio of maximum to minimum capacitance that varactor can provide
  - The quality factor of the varactor

PN Junction Varactor

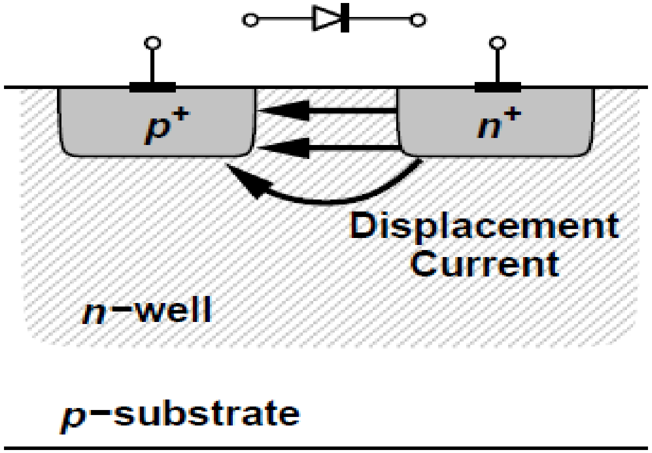


$$C_j = \frac{C_{j0}}{\left(1+\frac{V_D}{V_0}\right)^m}$$

where C_{j0} is the capacitance at zero bias voltage, V_0 the built-in potential and m is an exponent around 0.3 in integrated structure

- Note that junction varactor have a weak dependence of C_j upon V_D, because for $V_{D,max} = 1V$, then $C_{j,max}/C_{j,min} \approx 1.23$ (Low range)

Varactor Q Calculation Issues



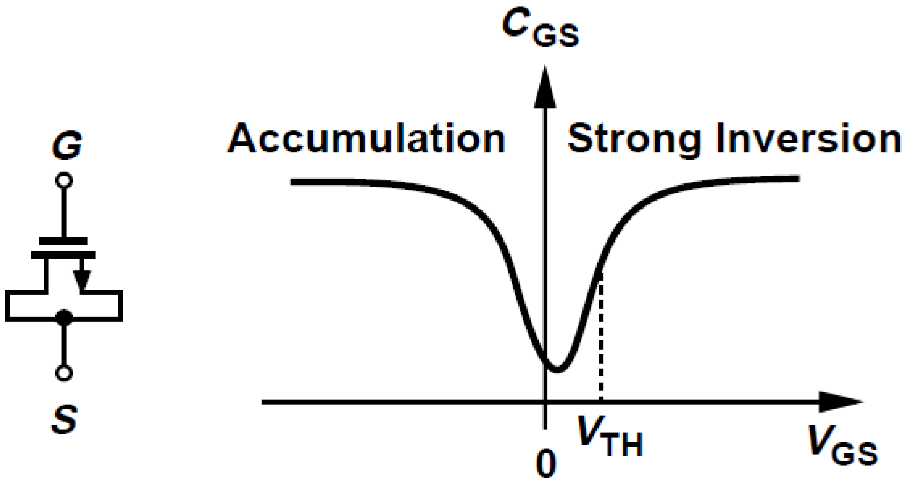
Current distribution in varactor

Q of varactor is obtained by measurement on fabricated structures

Difficult to calculate it because of the 2D current distribution

- As shown above, due to the two dimensional flow of current it is difficult to compute the equivalent series resistance of the structure
- N-well sheet resistance can not be directly applied to calculation of varactor series resistance

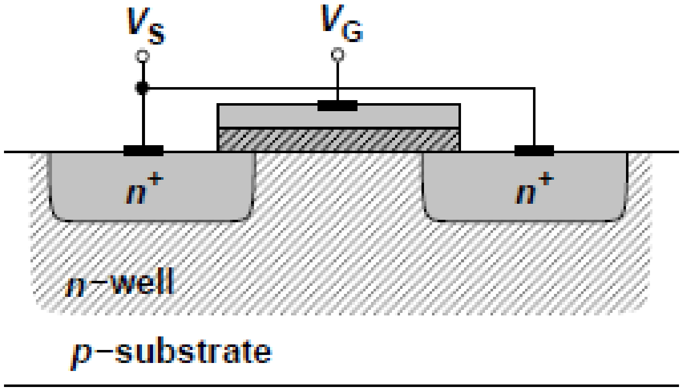
MOS Varactor

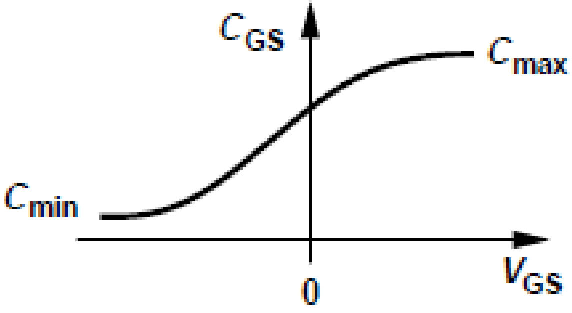


Variation of gate capacitance with V_{GS} for a regular MOS device

- A regular MOSFET exhibits a voltage dependent gate capacitance
- The non-monotonic behavior with respect to gate voltage limits the design flexibility

Accumulation Mode MOS Varactor

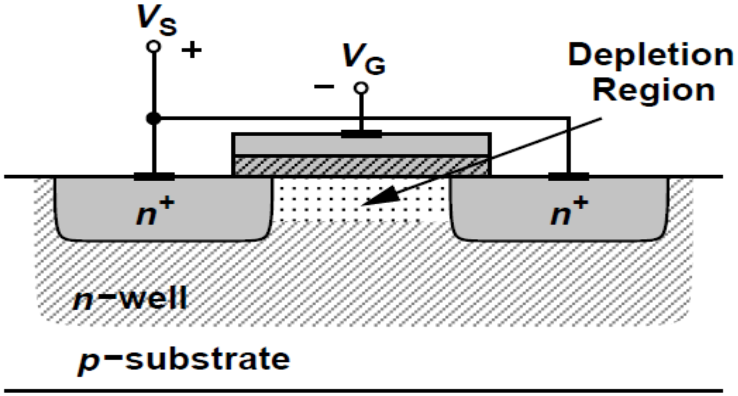




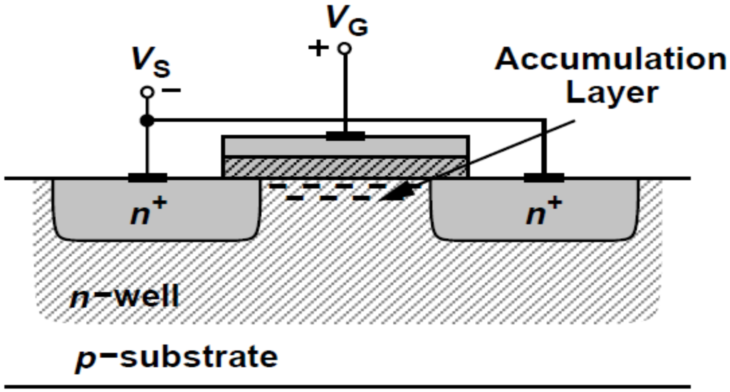
C/V characteristics of varactor

- Accumulation-mode MOS varactor is obtained by placing an NMOS inside an nwell
- The variation of capacitance with V_{GS} is monotonic
- The C/V characteristics scale well with scaling in technology
- Unlike PN junction varactor this structure can operate with positive and negative bias so as to provide maximum tuning range

Accumulation Mode MOS Varactor Operation

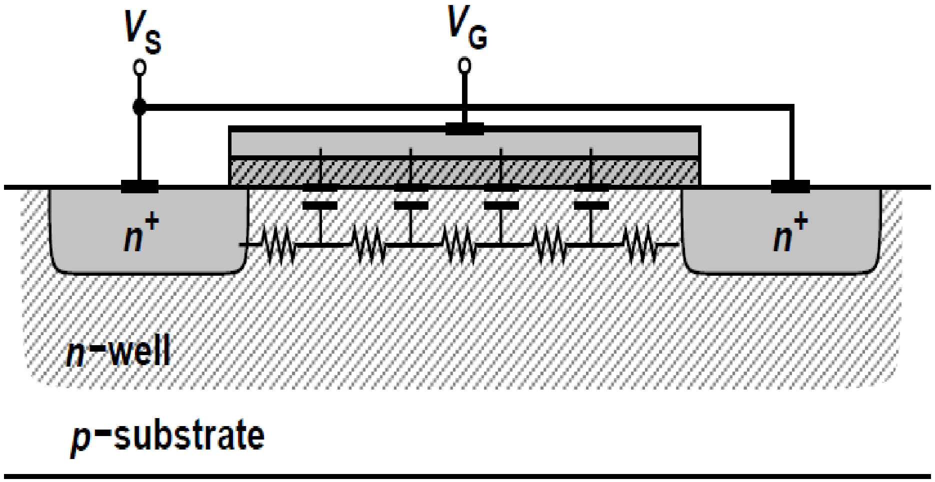


- $V_G < V_S$
- Depletion region is formed under gate oxide
- Equivalent capacitance is the series combination of gate capacitance and depletion capacitance

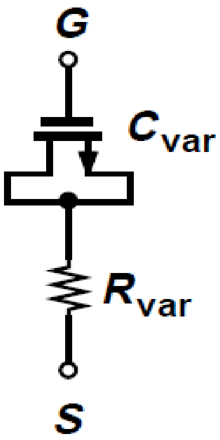


- $V_G > V_S$
- Formation of channel under gate oxide

Q of Accumulation mode MOS Varactor



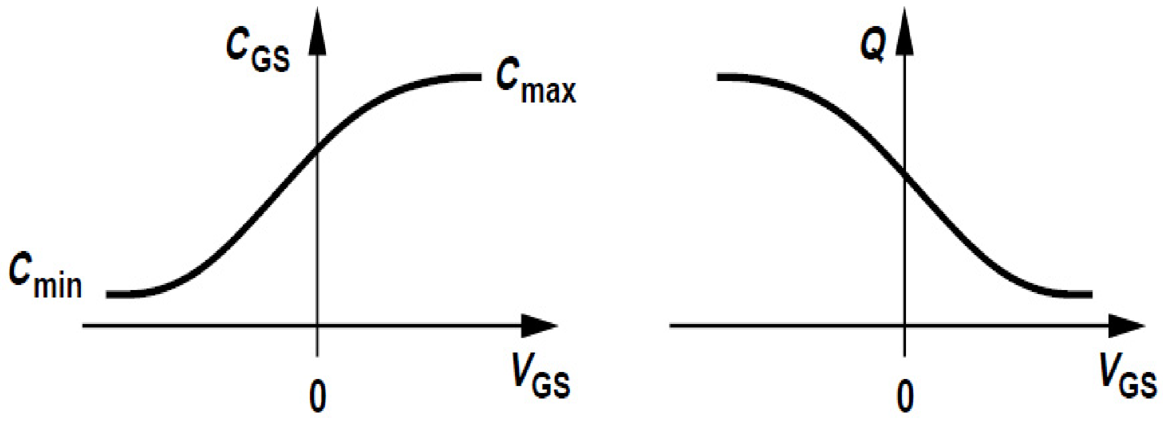
(a)



(b)

- The Q of the varactor is determined by the resistance between source and drain terminals
- Approximately calculated by lumped model shown in above

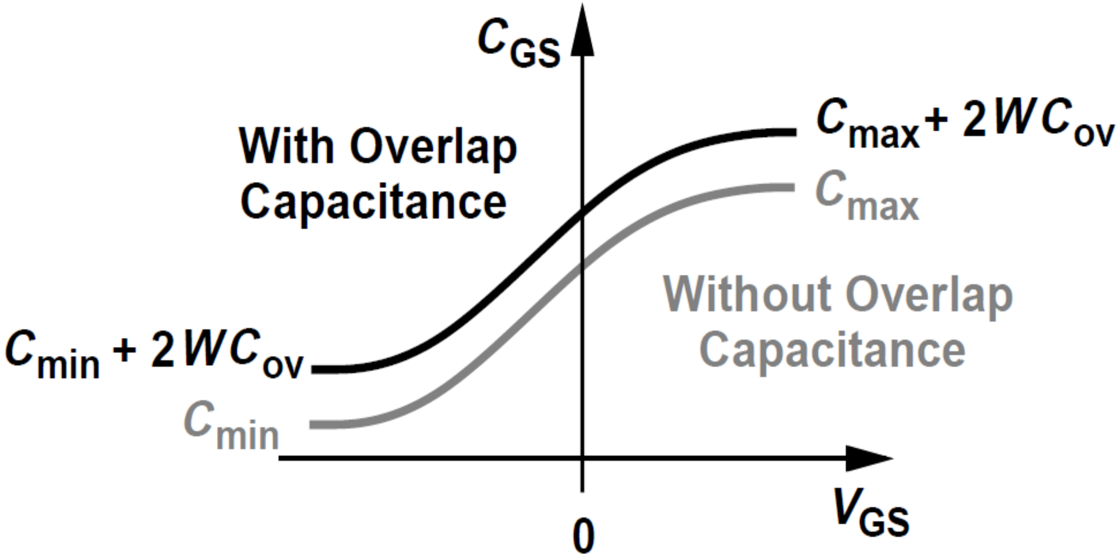
Variation of MOS Varactor Q with Capacitance



Variation of varactor Q with capacitance

- For C_{min}, the capacitance is small and resistance is large
- For C_{max}, the capacitance is large and resistance is small
- Above comments suggest that Q remains relatively constant
- In practice, Q drops as we increase capacitance from C_{min} to C_{max}, suggesting that relative rise in capacitance is greater than fall in resistance

Effect of Overlap Capacitance on Capacitance Range



- Overlap capacitance is relatively voltage independent.
- Overlap capacitance shifts the C/V characteristics up, yielding a ratio of

$$\frac{C_{\max} + 2WC_{ov}}{C_{\min} + 2WC_{ov}}$$

References

Most of this Chapter is based on Chapter 7 of Reference [1]

[1] B. Razavi, *RF Microelectronics*, 2nd ed. Pearson, 2012.