MICRO-461
Low-power Radio Design for the IoT

11. RF Power Amplifiers

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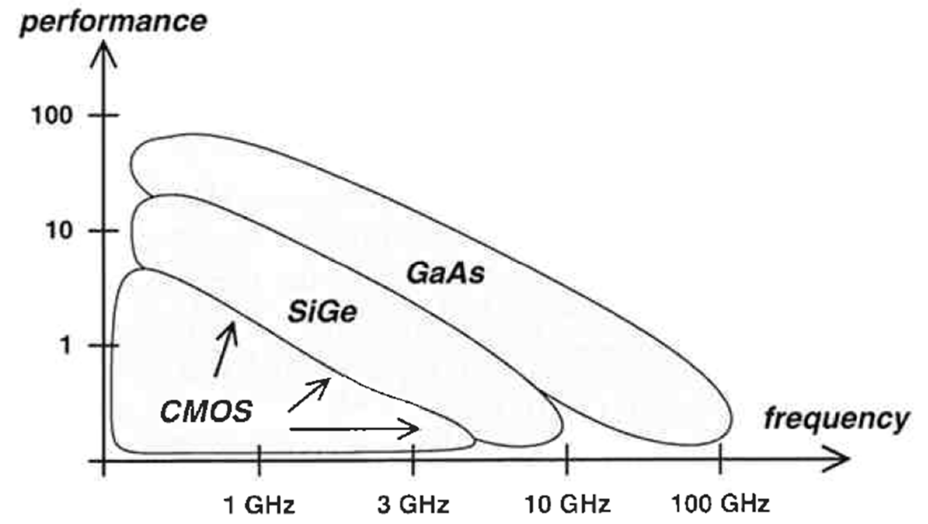
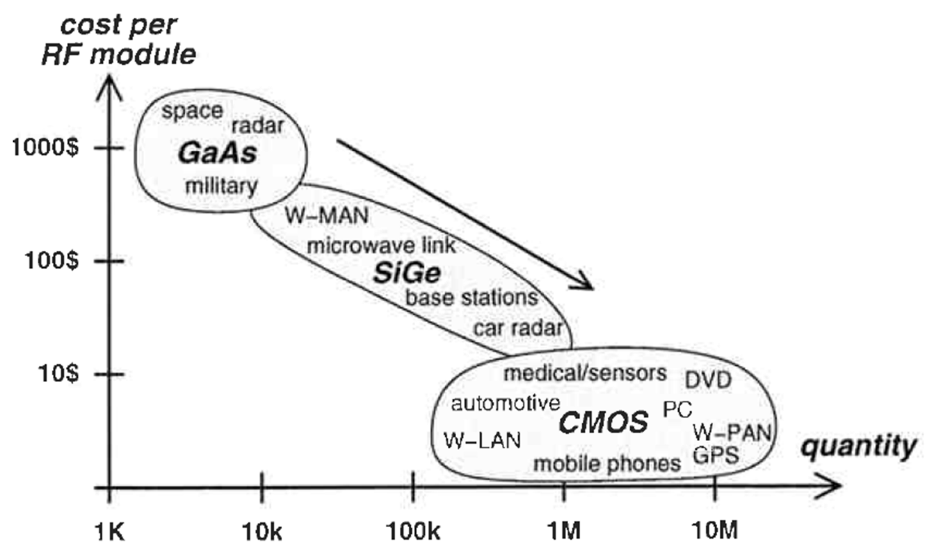
Outline

- Introduction and Definitions
- Basic Power Amplifiers
  - Linear Power Amplifiers – classes A, AB, B and C
  - Switching Power Amplifiers – classes D, E, (F)
- Linearization and Efficiency Enhancement Techniques

Introduction

- CMOS technology is not optimized for high-power and high-frequency operation
- The driver behind CMOS is the price and high level of integration
- For high-end applications (space, military) dedicated technologies are indispensable
- Mid-range applications are dominated by CMOS





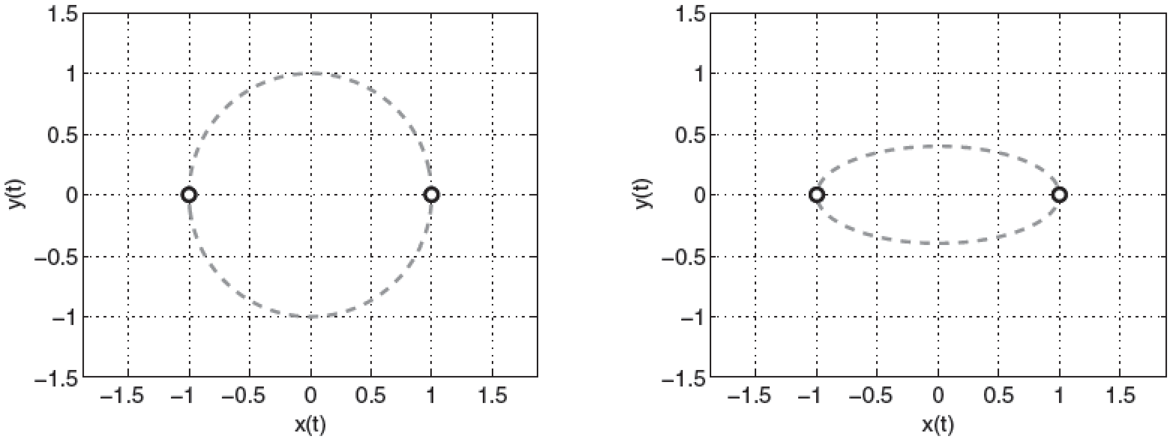
P. Reynaert and M. Steyaert, *RF Power Amplifiers for Mobile Communications*, Springer, 2006.

Introduction

- Most important aspects of power amplifiers:
  - **Output power** – Low supply voltage of deep submicron technology nodes makes it difficult to achieve power levels needed for some applications
  - **Efficiency** – The key metric of power amplifiers, determines autonomy of the system (the PA is usually the most power hungry block in the system)
  - **Linearity** – important for high-performance systems employing complex modulation schemes (QAM, OFDM etc.). Low power systems tend to use simpler schemes with no amplitude modulation in order to simplify implementation of power amplifiers
  - **Gain** – traditionally power gain, although in modern CMOS technologies can be replaced by driving requirements (input power cannot be defined for a purely capacitive load)

Signal Properties

- In order to optimize a power amplifier it is necessary to understand signal properties
- **Constant Envelope** – the envelope of the transmitted signal constant over time, possible to use a non-linear amplifier, typically more efficient – phase or frequency modulated signals
- **Non-Constant Envelope** – the signal envelope varies with time, linear power amplifier is necessary, typically less efficient

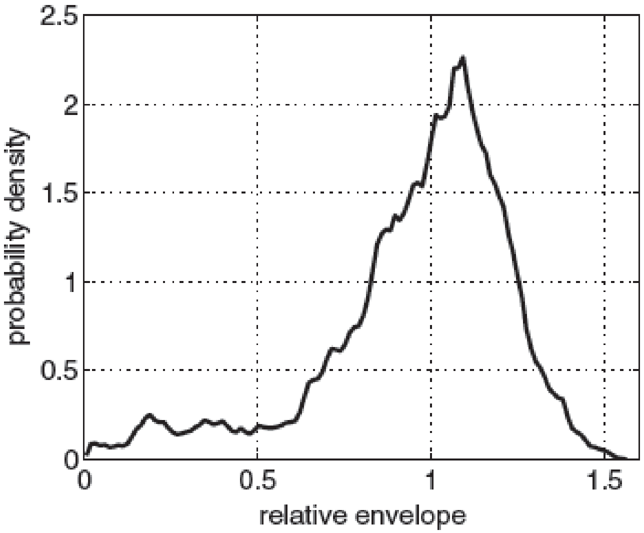


(a) constant envelope (b) non-constant envelope

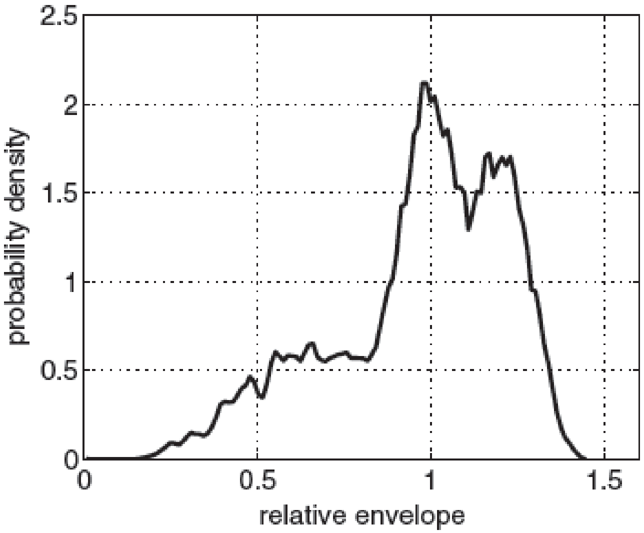
P. Reynaert and M. Steyaert, *RF Power Amplifiers for Mobile Communications*, Springer, 2006.

Signal PDF

- Amplitude variation can be quantified using **Peak-to-Average Power Ratio** (PAPR), defined as the ratio of maximum and average power
- A more complete description of amplitude modulation can be given using a PDF of the envelope signal
  - PDF of a constant envelope signal corresponds to a Dirac impulse



(a) QPSK



(b) $\pi/4$-QPSK

P. Reynaert and M. Steyaert, *RF Power Amplifiers for Mobile Communications*, Springer, 2006.

PA Definitions

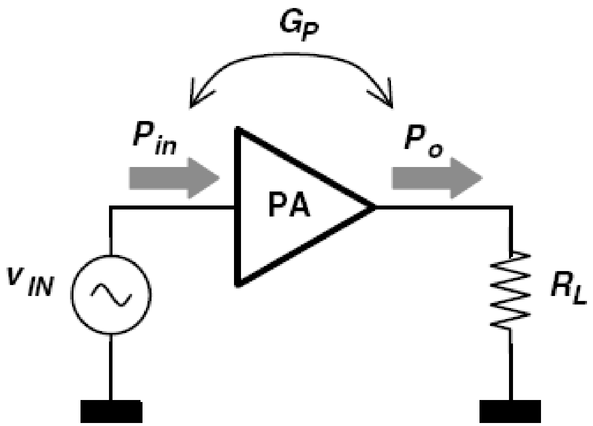
- **Output power** is the power delivered to the load, usually interested in maximum output power and average output power

$$P_{tot} = \langle p(t) \rangle = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} p(t) dt$$

$$P_o = \langle v_{out}(t) \cdot i_{out}(t) \rangle = \frac{\langle v_{out}^2(t) \rangle}{R_L} = \frac{V_{o,rms}^2}{R_L}$$

- **Power gain** – traditionally used for PAs with a real input impedance. For CMOS PAs up to 10 GHz input impedance is capacitive and hence input power cannot be defined

$$G_{p,dB} = 10 \log \frac{P_o}{P_{in}}$$



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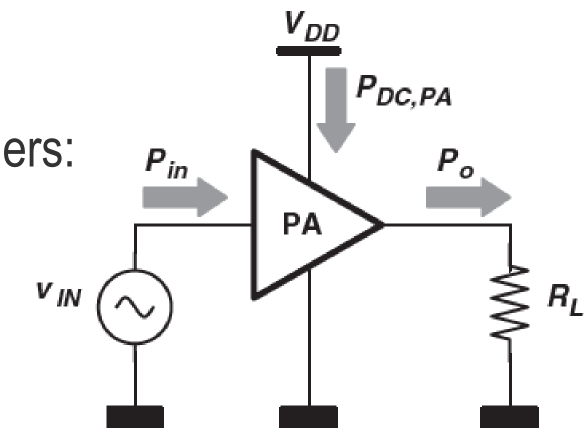
PA Definitions



- Different ways to define efficiency of power amplifiers:
  - **Drain efficiency**:

$$\eta_d = \frac{P_o}{P_{DC,PA}}$$

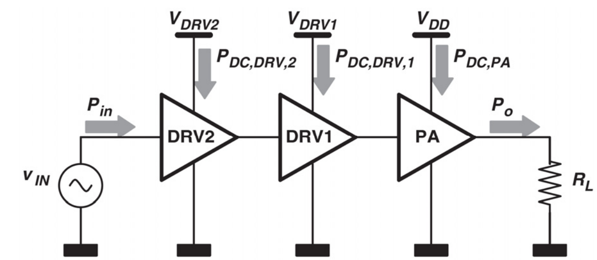
  - Note that only power at the fundamental frequency is relevant
  - It is possible to define conversion efficiency as a ratio of total output power to the DC power consumption
  - **Overall efficiency**:

$$\eta_{oa} = \frac{P_o}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,DRV,i}}$$

Power dissipated in the driver stages

Power Added Efficiency (PAE):

$$PAE = \frac{P_o - P_{in}}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,DRV,i}}$$



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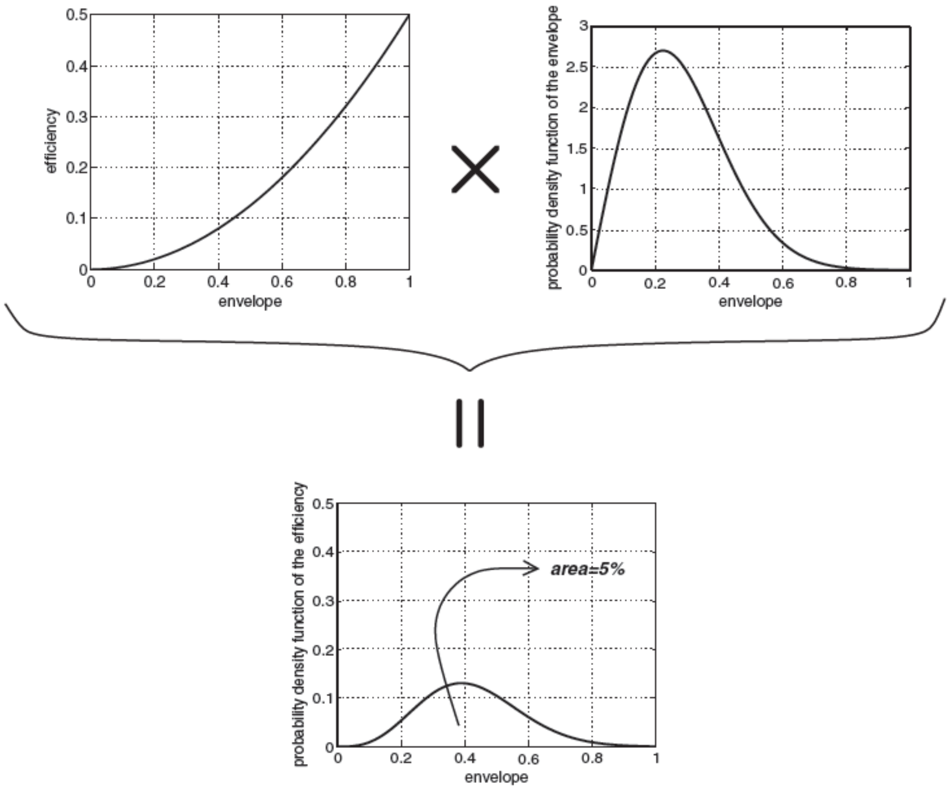
Efficiency Optimization

- If the PDF of the signal is known and drain efficiency as a function of signal envelope (amplitude) is known then average drain efficiency can be calculated as:

$$\eta_d = \int_0^{A_{max}} \eta_d(A) \cdot p(A) \cdot dA$$

- As a general rule efficiency and linearity are contradictory requirements
  - Nonlinear amplifiers typically exhibit higher efficiency



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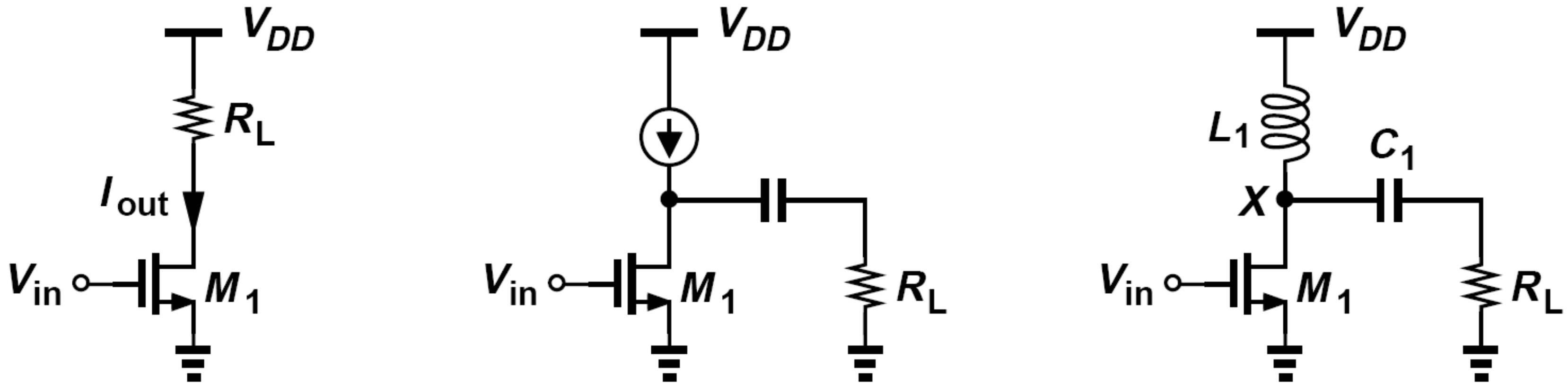
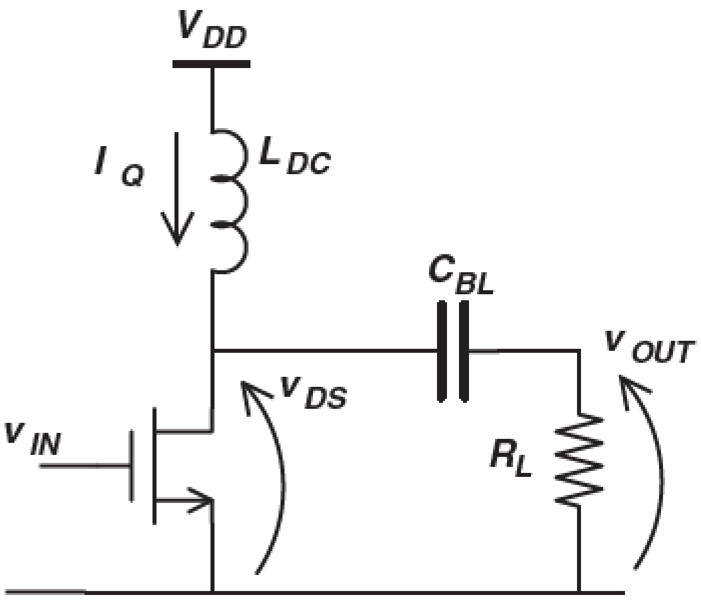
Common Source Amplifier



- All the power amplifiers that will be mentioned today use a common source configuration
- How are they different to common source amplifiers you have seen before? Here we are talking about large signals! The aim is to maximize efficiency and output power
- Purely resistive load limits achievable amplitude to $V_{DD}/2$ and efficiency to 25%
- Can we do better?

Class A Power Amplifier

- Instead of a resistor a large inductor is used in the drain of the transistor
  - Short circuit for DC, and open for AC signals (RF choke)
- DC value of the drain voltage is equal to V_{DD}
- Output signal can swing from 0 to $2V_{DD}$
- Load separated by a DC blocking capacitor
  - Short circuit for AC signals, open for DC
- Transistor is assumed ideal:
  - Saturation voltage is 0
- Passive components assumed ideal
  - No losses



Class A Power Amplifier

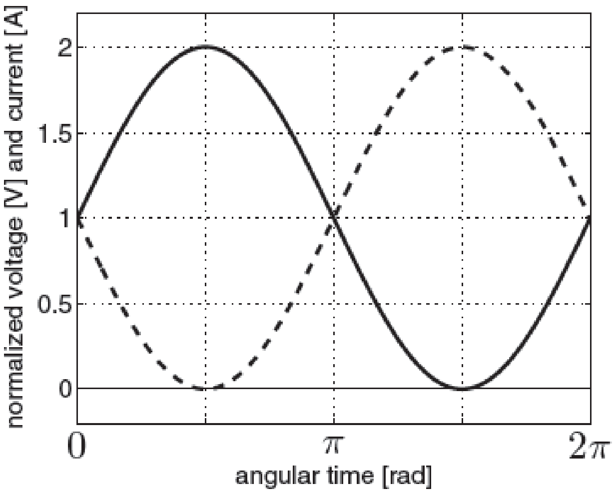
- Output power of a class A amplifier and DC consumption are given by:

$$P_o = \frac{V_o^2}{2R_L} \quad , \quad P_{DC} = V_{DD} I_{DC} = \frac{V_{DD}^2}{R_L}$$

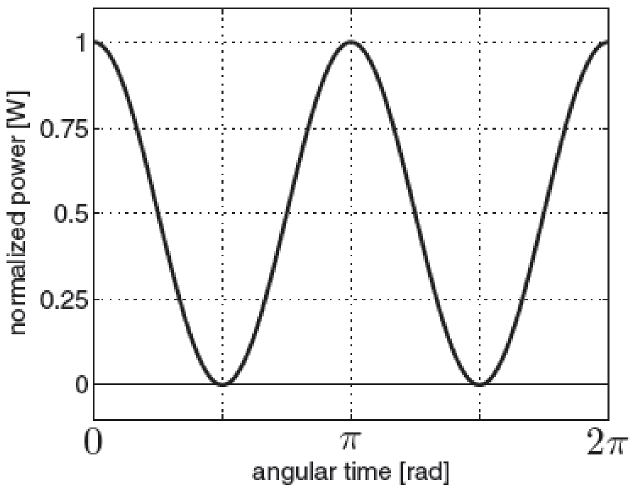
- The theoretical drain efficiency is then given by:

$$\eta_d = \frac{P_o}{P_{DC}} = \frac{1}{2}\left(\frac{V_o}{V_{DD}}\right)^2 = 0.5 \quad \text{if} \quad V_o = V_{DD}$$

- Maximum efficiency of a class A amplifier is 50%
- Reduces with square of the output amplitude
- Highest linearity



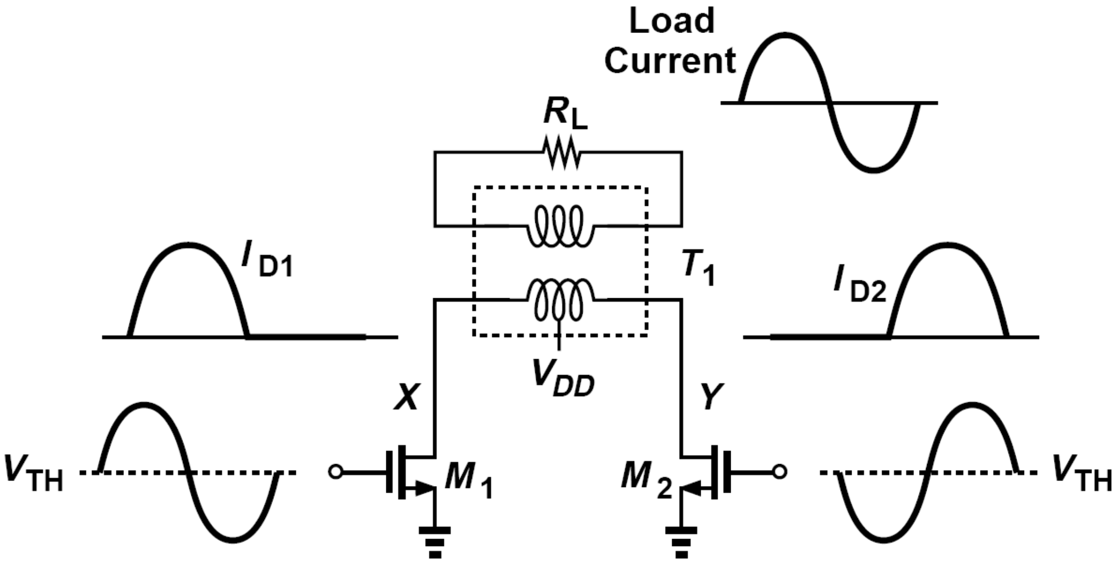
(a)



(b)

Class B Power Amplifier

- Class B power amplifier – each transistor only conducts half the time
- Idea: increase the efficiency by switching transistors off for a period of time



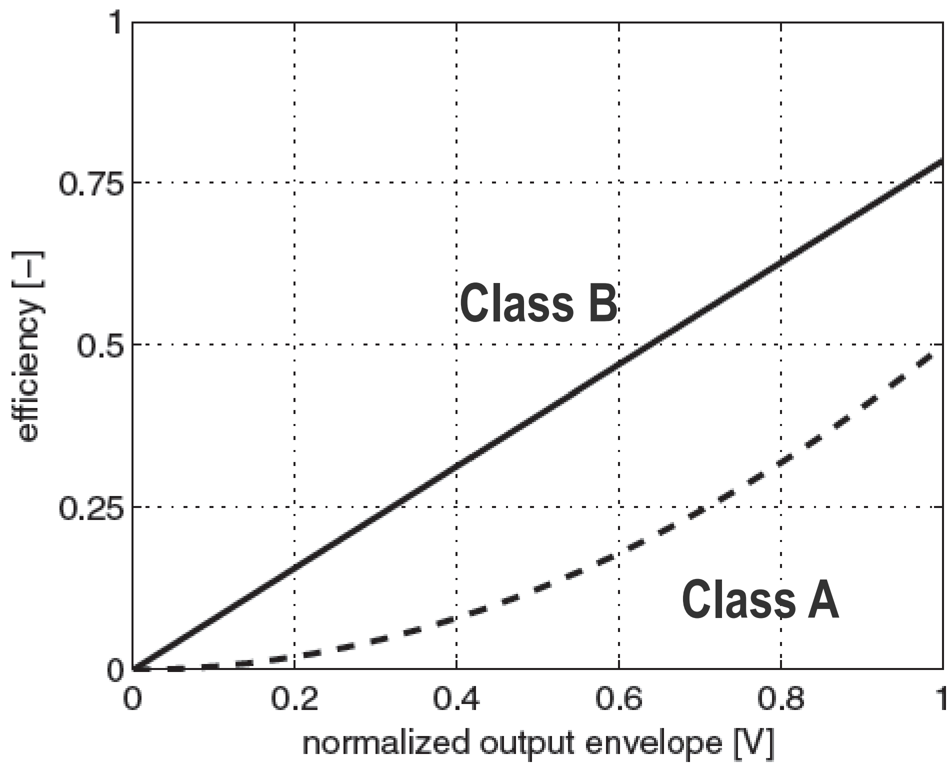
- DC power, output power and efficiency:

$$P_{DC} = \frac{2}{\pi} I_P V_{DD}, \qquad P_o = \frac{1}{2} I_P^2 R_L, \qquad \eta_D = \frac{\pi}{4} \frac{V_o}{V_{DD}}$$

- Maximum efficiency around 78.4%

Efficiency of class B

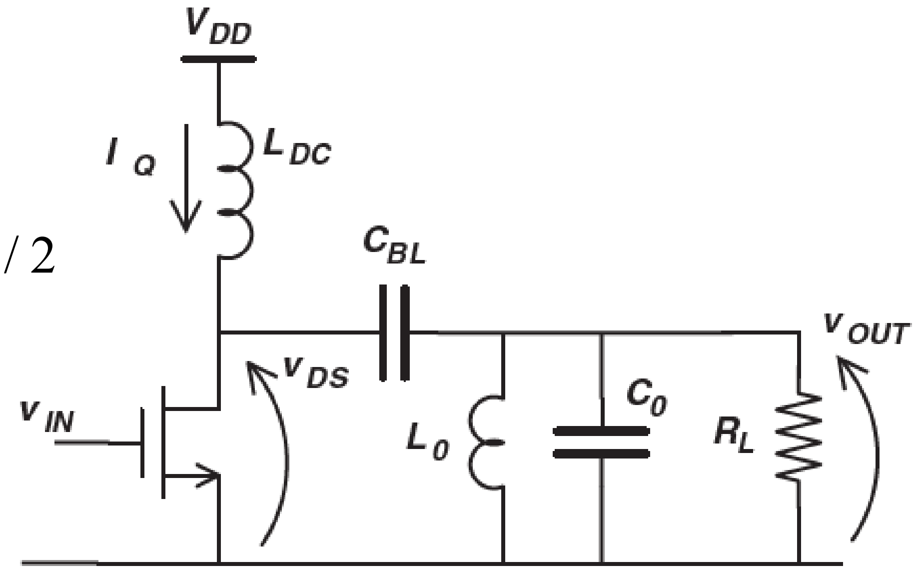
- Another advantage of class B is that the output efficiency is proportional to V_o
- Efficiency drops slower for power back-off
- Better characteristic for amplitude modulated signas



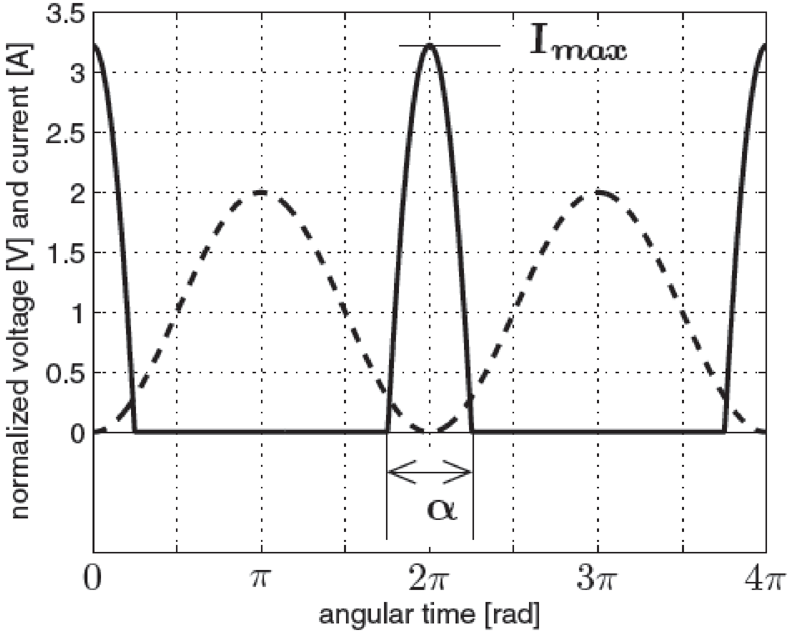
Reduced Conduction Angle

- Reducing the conduction angle from 2π to π leads to an increase in efficiency
- An arbitrary conduction angle can be chosen
- Determined by the bias of the transistor
- Assume the current pulse is shaped like a part of a sine wave
  - This waveform generates higher harmonics
  - Output resonant load acts as open for the fundamental and short for all higher harmonics
  - Output voltage is a sine
  - Drain voltage is a sine

$$i_{DS}(\theta) = \begin{cases} I_{DC} + I_{pk}\cos(\theta) & -\alpha/2 \le \theta \le \alpha/2 \\ 0 & \text{elsewhere} \end{cases}$$



Reduced Conduction Angle

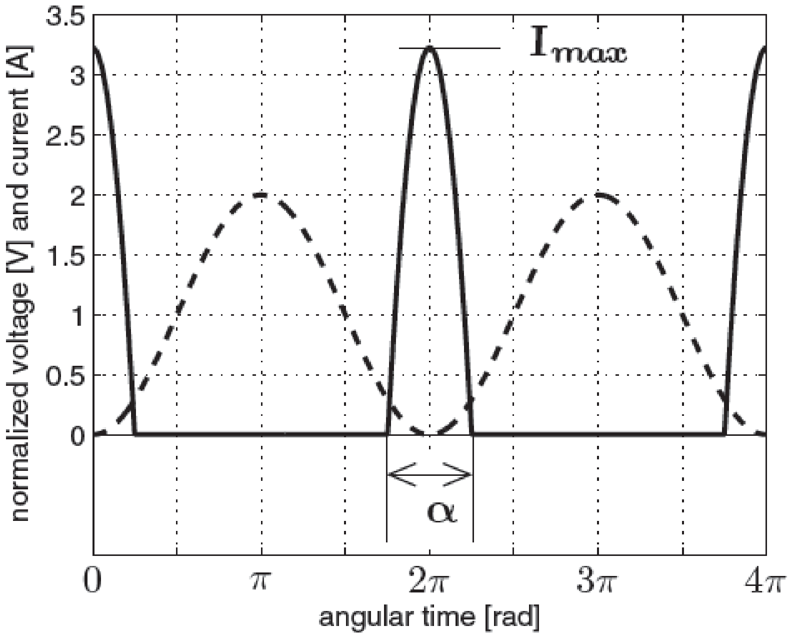


- For a given current, magnitude of the n-th harmonic can be calculated as:

$$I_n = \frac{1}{\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} \left[\cos(\theta) - \cos(\alpha/2)\right] \cos(n\theta) d\theta$$

$$I_1 = \frac{I_{max}}{2\pi} \frac{\alpha - \sin(\alpha)}{1 - \cos(\alpha/2)}$$

Reduced Conduction Angle



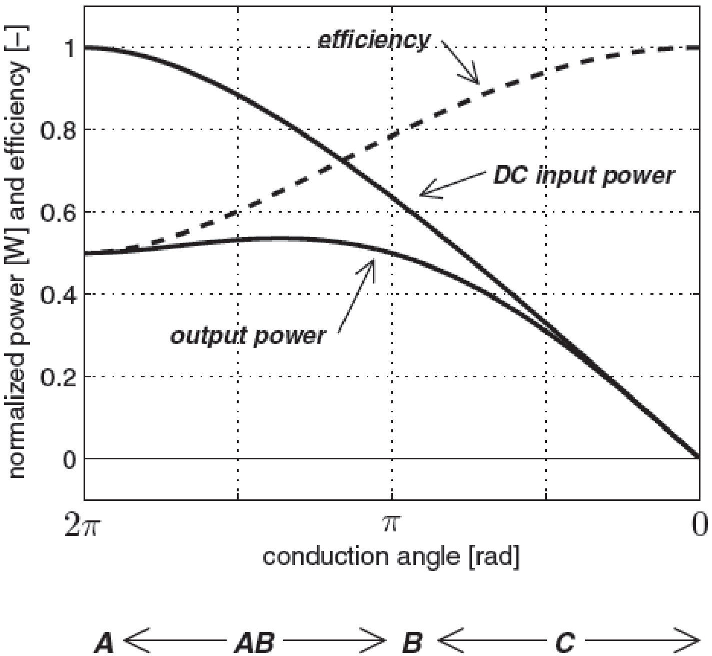
- DC current is given by:

$$
\begin{aligned}
I_{DC} &= \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)}\left[\cos(\theta) - cos(\alpha/2)\right] d\theta \\
&= \frac{I_{max}}{2\pi}\,\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}
\end{aligned}
$$

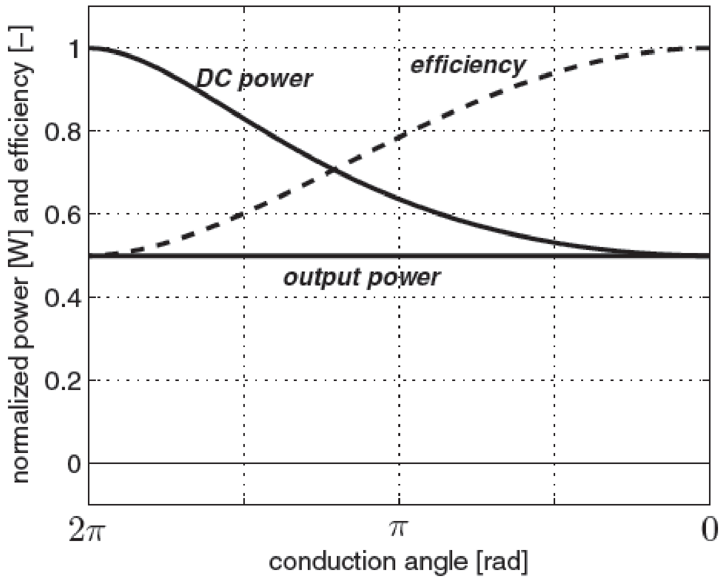
Reduced Conduction Angle

- It is then possible to calculate the theoretical efficiency for a given conduction angle and compare different classes of PAs

Normalized for constant I_{max}



Normalized for constant P_{out}

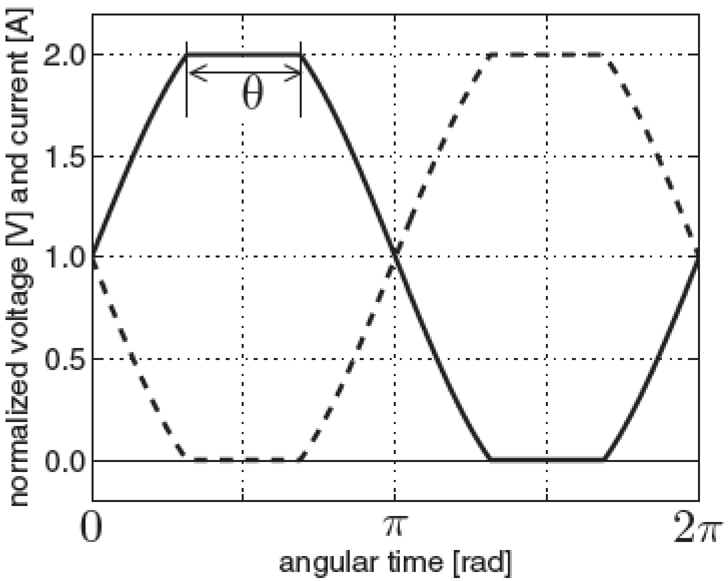


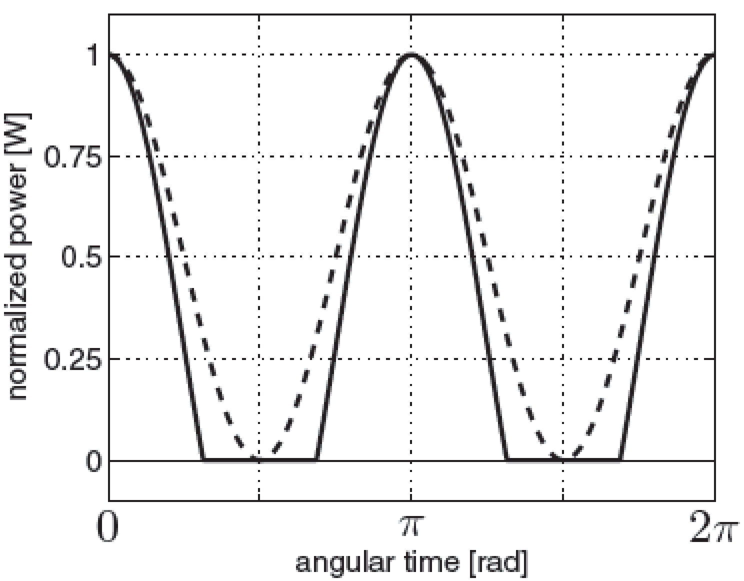
Reduced Conduction Angle

- The efficiency increases as the conduction angle decreases, however:
  - Output power decreases - for a zero conduction angle the output power tends to zero
  - Driving requirements increase - larger signal swing is needed at the gate (to generate a larger current pulse) resulting in increased power consumption of the driver - important for low power transmitters
  - For a capacitive load dissipated power is proportional to $\sim fCV^2$
  - Increases with the input amplitude - higher for a lower conduction angle
- Class C is rarely used in practice due to low output power and high driving requirements

Saturated Class A

- So far the assumption was that the maximum amplitude is V_{DD}
- Assume we start from the class A amplifier and increase the drive so that the drain voltage starts to clip
- As the driving signal increases the clipping angle increases
- In the limit case the drain current and voltage become square waves





Saturated class A

- In the limiting case there is no overlap between the drain current and the drain voltage - **no losses in the transistor**
- But the output voltage contains higher harmonics → loss of efficiency
- Total output power and DC power are given by:

$$P_{o,tot} = \frac{V_{DD}^2}{R_L}$$

- Fundamental output voltage is given by:

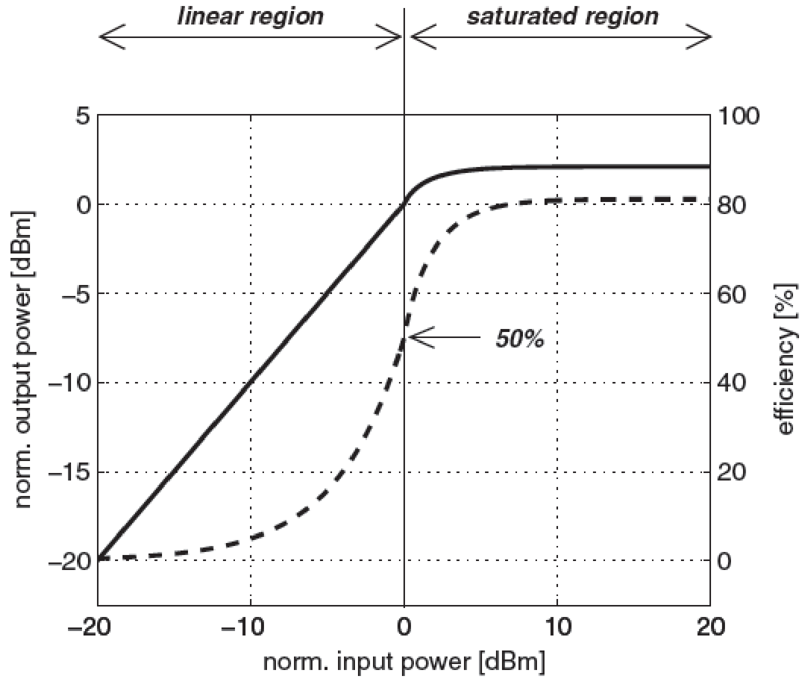
$$V_o = V_{DD} \cdot 4/\pi$$

- Resulting in output power given by:

$$P_o = \frac{(V_{DD} \cdot 4/\pi)^2}{2R_L}$$

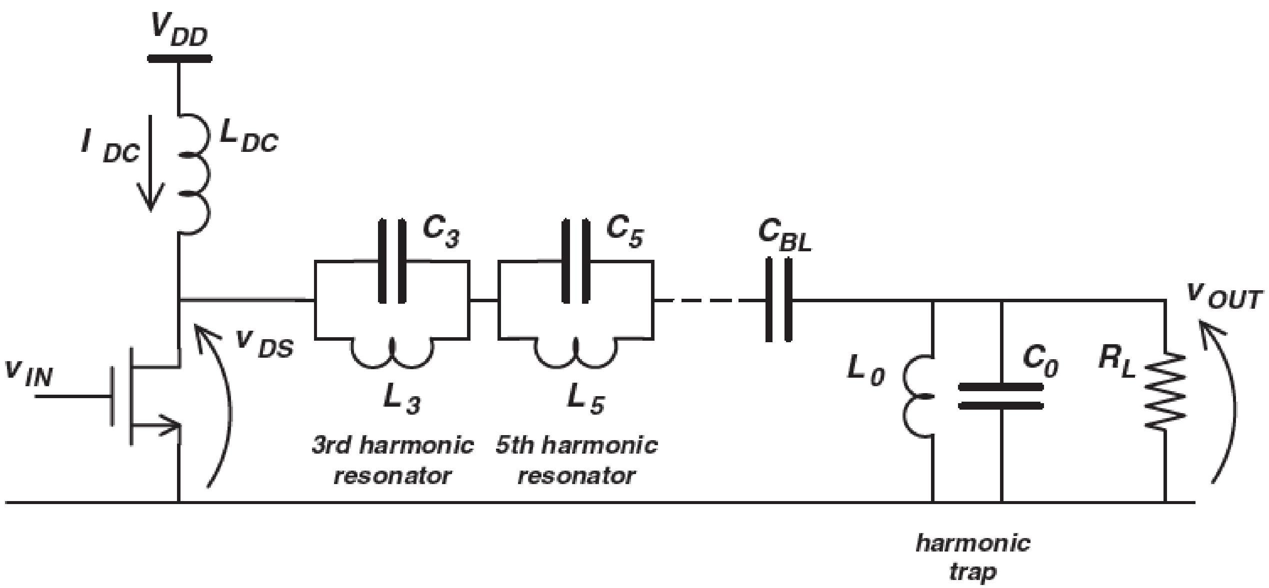
- And finally a maximum efficiency of:

$$\eta = \frac{(4/\pi)^2}{2} = 8/\pi^2 \approx 81\%$$



Class F

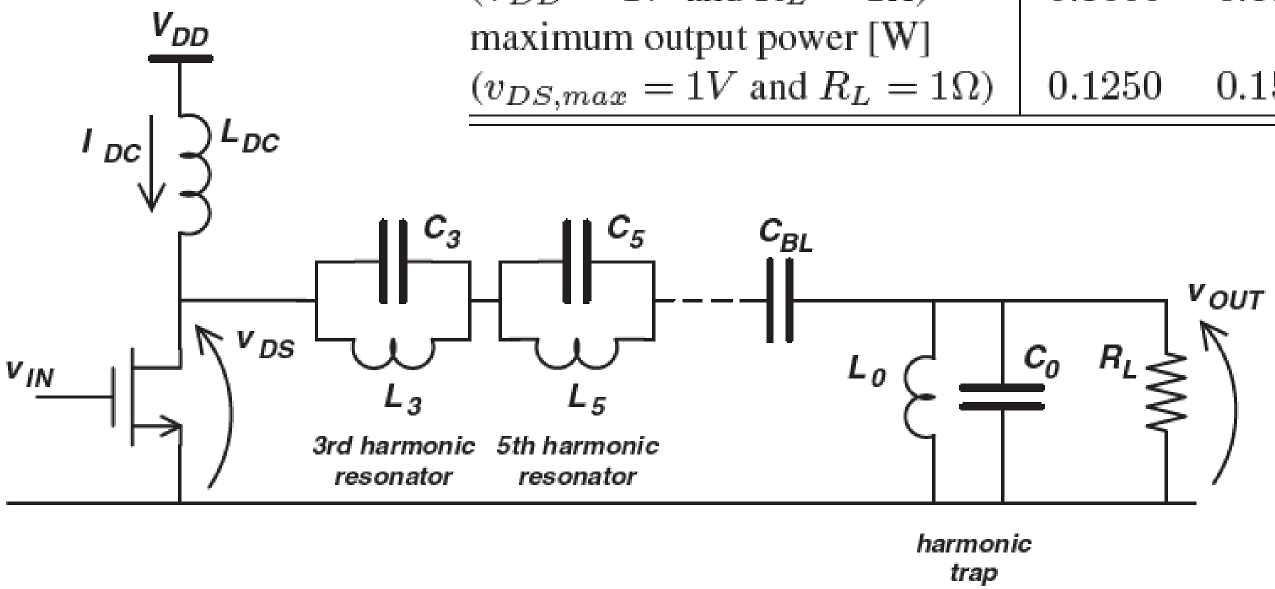
- Saturated class A amplifier eliminates losses in the transistor, but power is lost in output harmonics resulting in 81% efficiency
- Losses in higher harmonics can be avoided by introducing a tuned load that removes higher harmonics and shapes the drain current and voltage
- In this way a class F amplifier is derived



Class F

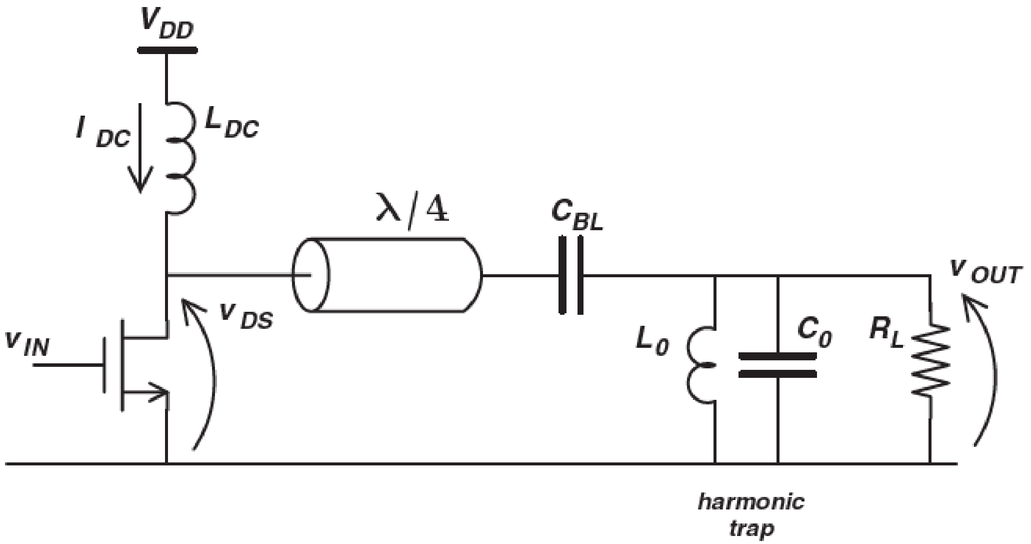
- Class F can achieve the theoretical drain efficiency of 100%
- Efficiency improves with addition of each resonator

included harmonic		3	5	∞
Class	B	F3	F5	D
peak efficiency	78.5%	88.4%	92.0%	100%
normalized output power [W] ($V_{DD} = 1V$ and $R_L = 1\Omega$)	0.5000	0.6328	0.6866	0.8106
maximum output power [W] ($v_{DS,max} = 1V$ and $R_L = 1\Omega$)	0.1250	0.1582	0.1717	0.2026



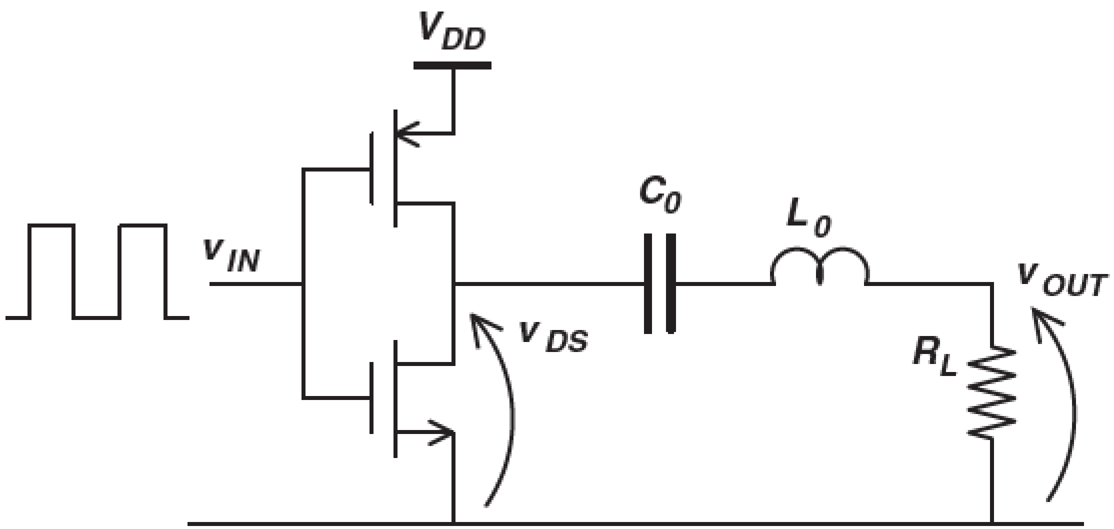
Class F

- Class F is impractical due to a large number of passive components
- In practice all of these components will add losses
- Difficult to integrate on chip
- Instead of using a large number of resonators a transmission line can be used
  - Again, due to length of transmission lines, impractical for frequencies below 10 GHz
  - Transmission line also introduces some losses



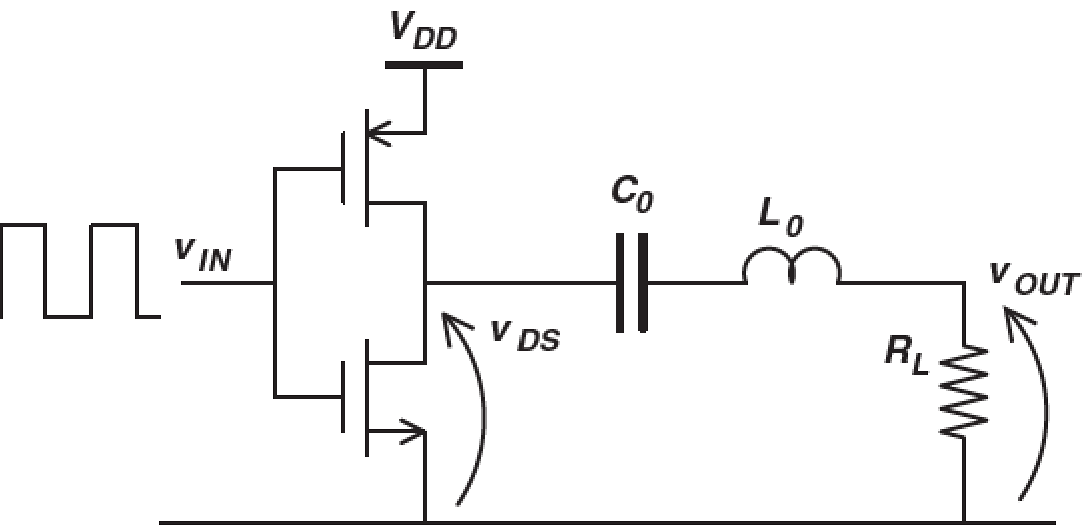
Class D

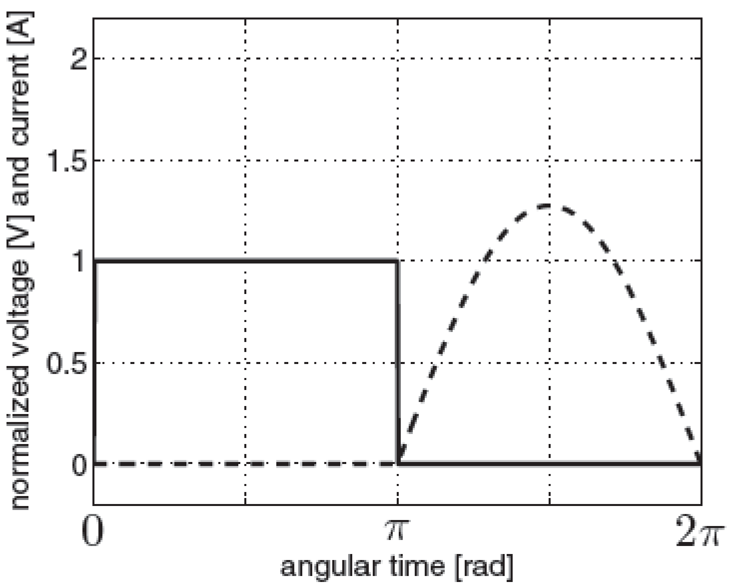
- Class F is not a switching amplifier, only when an infinite number of resonators are used and the drain voltage is square a transconductor can be replaced with a switch
- Class D is the first real switching amplifier
- Two transistors are needed a PMOS and an NMOS
- Essentially an inverter with a resonant load



Class D

- If the switches are ideal drain voltage will be a square wave
- Resonant load removes all the higher harmonics from the output current
- As a result output current is a sine
- Ideally transistor losses are eliminated and output efficiency reaches 100%





Class D

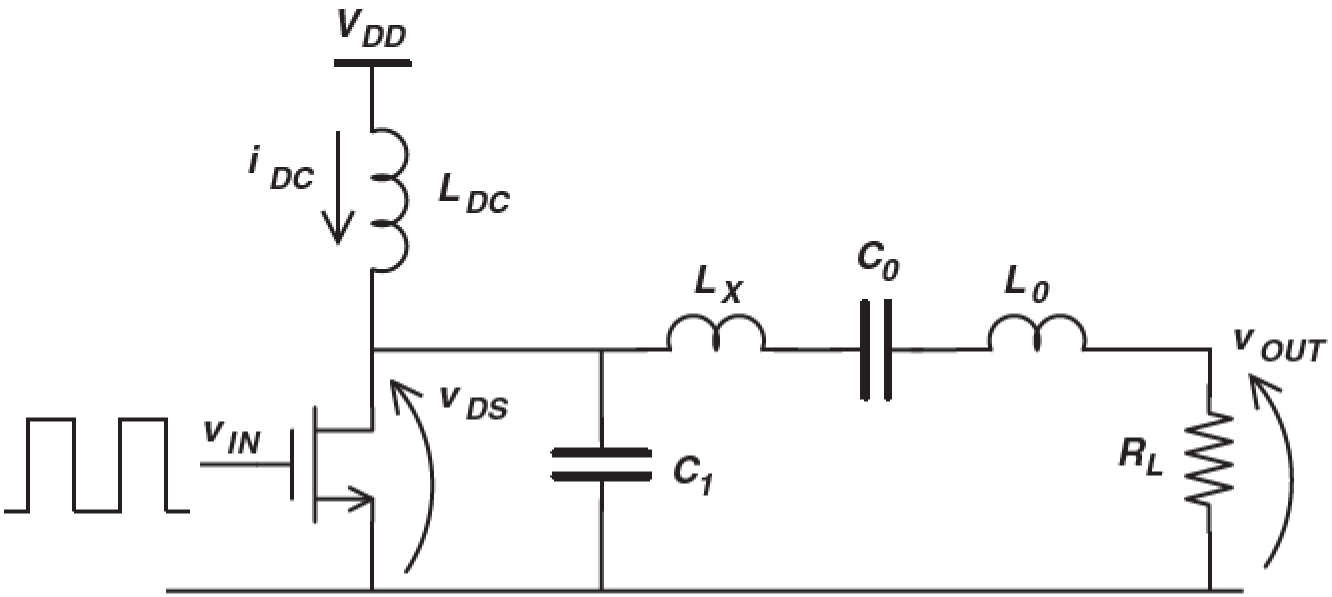
- Although theoretically class D reaches 100% efficiency there are several issues:
- Driving requirements - two transistors need to be driven, more power dissipated in the driving stage

$$P_{diss} = \frac{1}{2} f C V^2$$

- At the same time efficiency of the class D is inversely proportional to the switch resistance, meaning that the output transistors need to be wide and hence input capacitance will be large
- Output parasitic capacitance is constantly charged and discharged by the two switches resulting in losses
- Class E solves some of these issues

Class E

- This discussion will be limited to qualitative analysis of the class E amplifier
- In general class E is analyzed entirely in the time domain
- Requires solving nonlinear differential equations
- Capacitance C_1 can be used to absorb the parasitic drain capacitance
- Only one switching transistor needed
- Achieves a theoretical efficiency of 100%

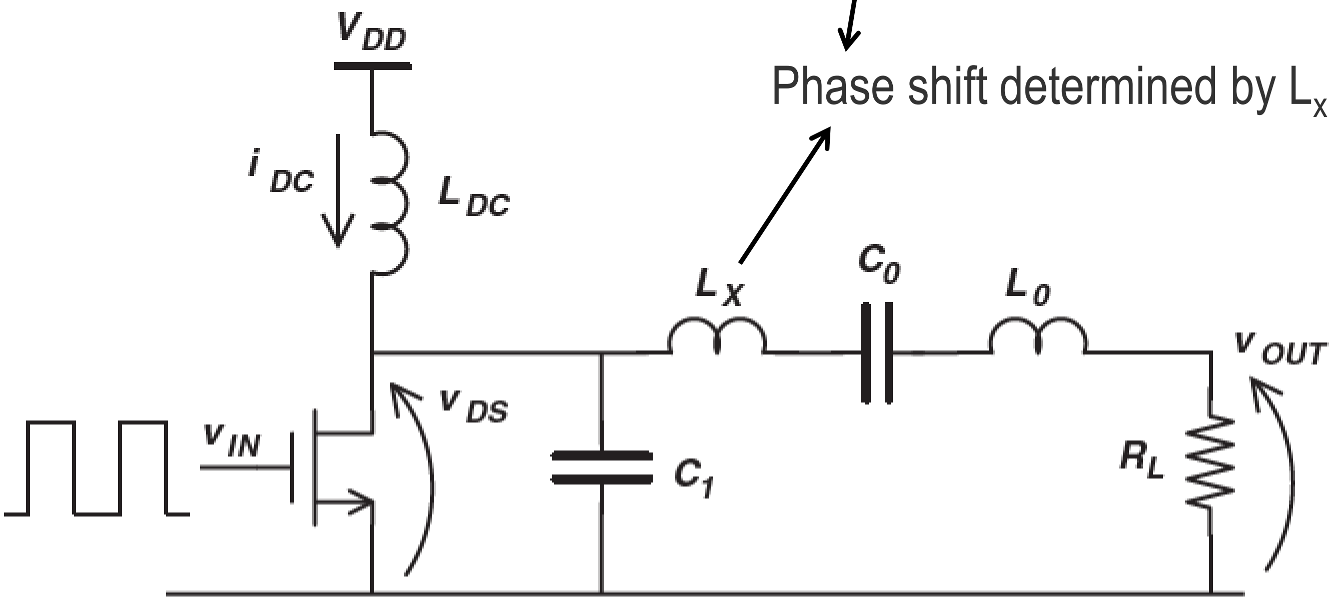


Class E

- To understand the operation of a class E amplifier we must make some assumptions
- The output current is a sine
- Resonator C_0 L_0 removes all the higher harmonics
- Since the RF choke current is constant, when the switch is open capacitor current is given by:

$$i_{C_1}(t) = I_{DC} - I_o \sin(\omega t + \varphi)$$

Phase shift determined by L_x

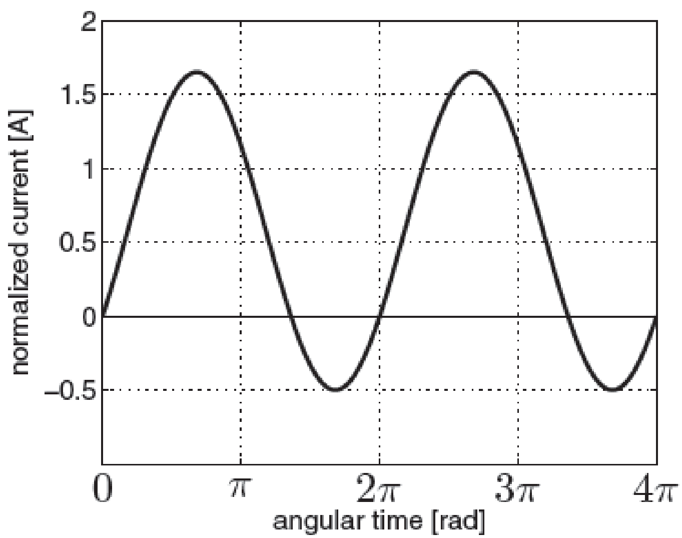


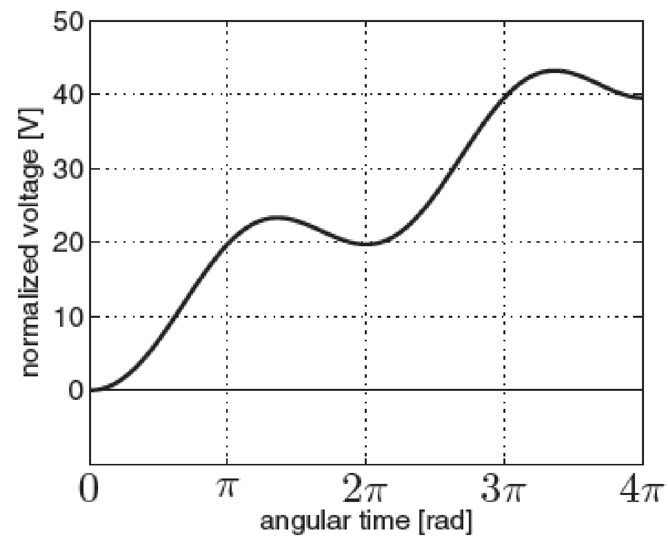
Class E

- When the switch is open the capacitor voltage grows according to:

$$\begin{aligned} v_{C_1}(t) &= \frac{1}{C_1}\int_0^{\infty}\left(I_{DC} - I_o \sin(\omega t + \varphi)\right) dt \\ &= \frac{1}{C_1}\left(I_{DC}\cdot t + \frac{I_o}{\omega}\cdot \cos(\omega t + \varphi)\right) + K_0 \end{aligned}$$

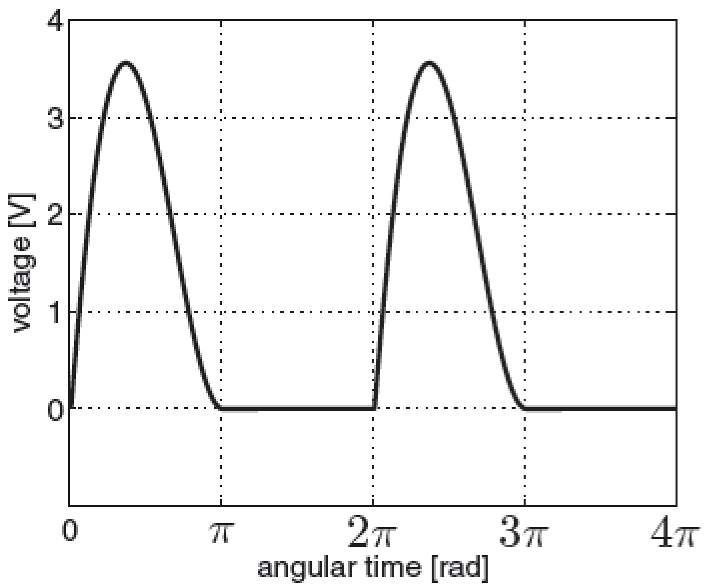
- It is interesting to observe the behavior of v_C from π to 2π - start and end value are the same

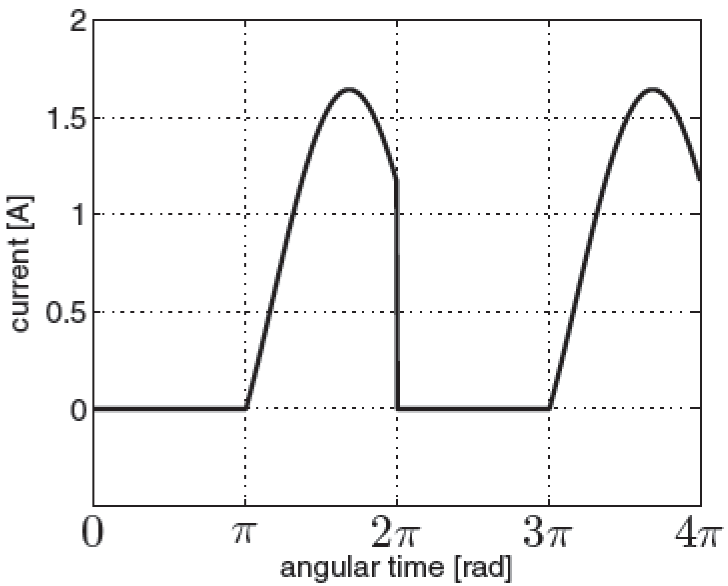




Class E

- If the switch is open and closed in precisely the right moments the capacitor voltage will be 0
- This is known as the Zero Voltage Switching (ZVS) and eliminates losses on C_1
- In addition, if the first derivative of the drain voltage is also 0 sensitivity to component values is reduced
- Ideal drain voltage and current are shown below:





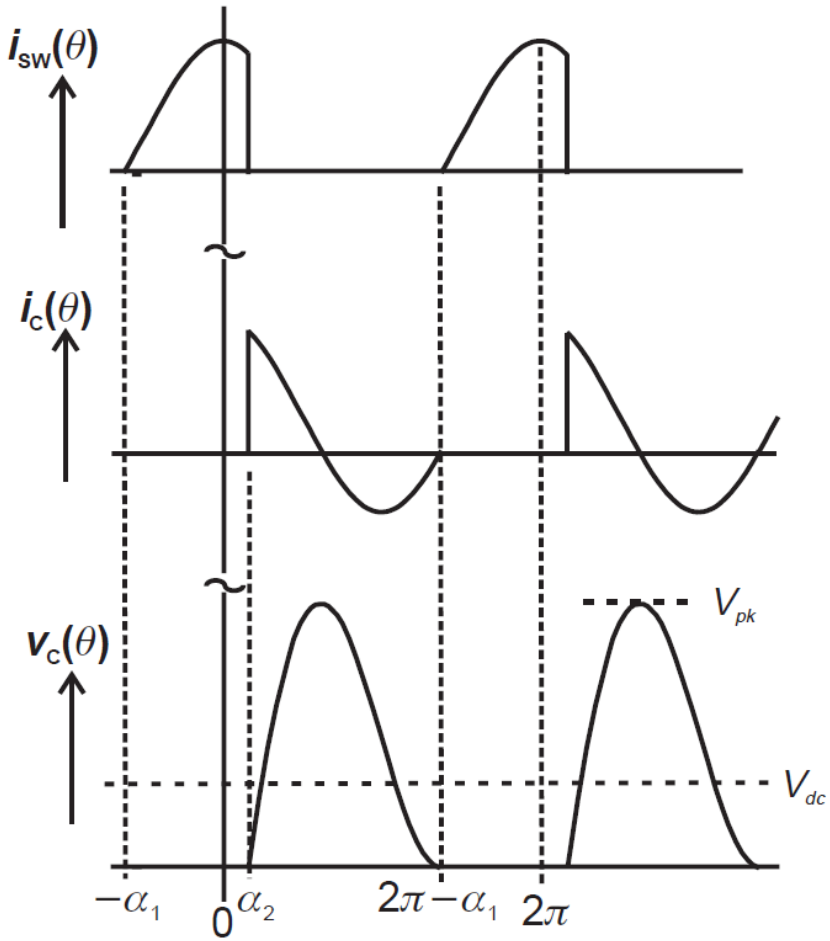
Class E

- Analytical derivation is somewhat complex but can be done for a case with lossless passive components
- Expressions for components and output power are then given by:

$$C_1 = \frac{8}{\pi(\pi^2+4)}\frac{1}{\omega R_L} \approx 0.1836\frac{1}{\omega R_L}$$

$$L_x = \frac{\pi(\pi^2-4)}{16}\frac{R_L}{\omega} \approx 1.1525\frac{R_L}{\omega}$$

$$P_o = \frac{8}{\pi^2+4}\frac{V_{DD}^2}{R_L} \approx 0.5768\frac{V_{DD}^2}{R_L}$$

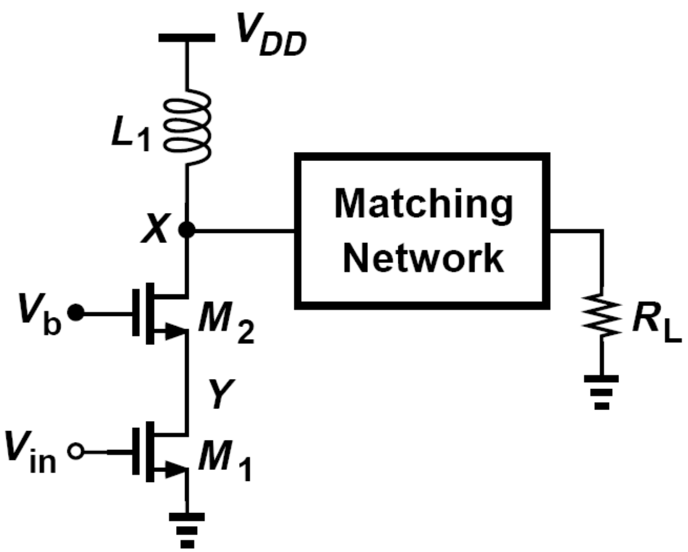


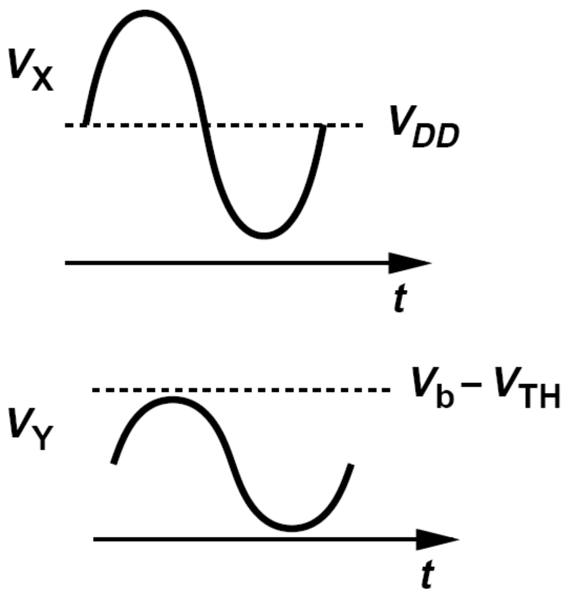
Class E

- One known issue with class E power amplifier is that the drain voltage goes up to almost $4V_{DD}$
- Might cause reliability issues if care is not taken
- Good news is that the current through transistor is 0 when the voltage is high
- Highest efficiency in practical applications
- Also highly nonlinear, cannot be used for amplitude modulated signals…
  - …at least not without some special techniques that will be discussed later

Cascode PA

- Output transistors can be stacked to provide a larger output voltage range
- Output voltage is split between the two transistors - supply can be increased
- Possible to us a thick gate transistor for the cascode (higher oxide breakdown voltage)
- Possible to stack several devices





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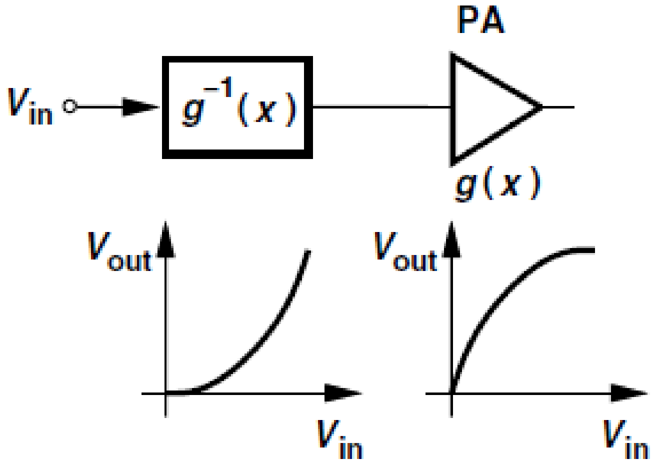
Efficiency Enhancement and Linearization

- Predistortion
- Adaptive Biasing
- Envelope tracking
- Doherty Amplifier
- Outphasing
- Envelope Elimination and Restoration (Polar Amplifier)
- Digitally controlled PA

Predistortion

- Most PAs (even the ones we called linear) have a non linear relation between the input and output signal
- In order to provide good linearity the input signal can be predistorted
- Distortion that negates the PA nonlinearity is intentionally introduced to the signal to provide a linear overall characteristic
- The PA nonlinearity needs to be known
- If this is not the case, or if PA characteristic changes over time (or temperature) feedback techniques need to be used

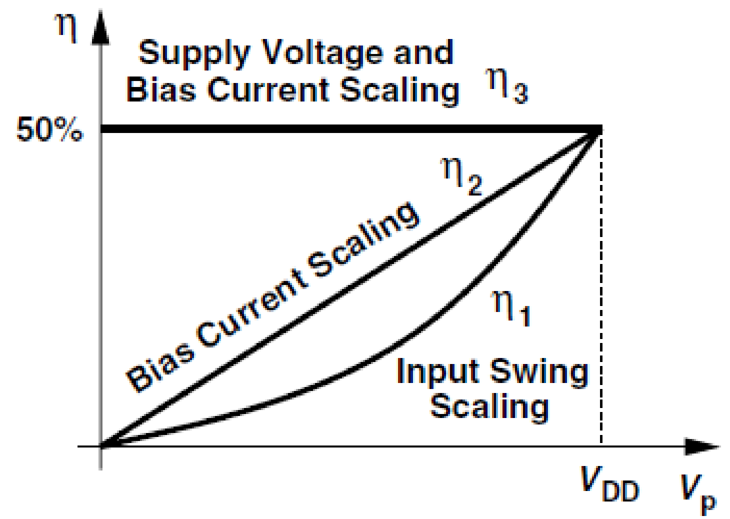


Adaptive Bias

- If a class A input signal amplitude decreases, output amplitude will decrease as well
- If the supply voltage and bias current remain the same, the efficiency drops with the square of output voltage as shown before
- If the bias current of the class A amplifier scales with the output voltage the efficiency will scale as:

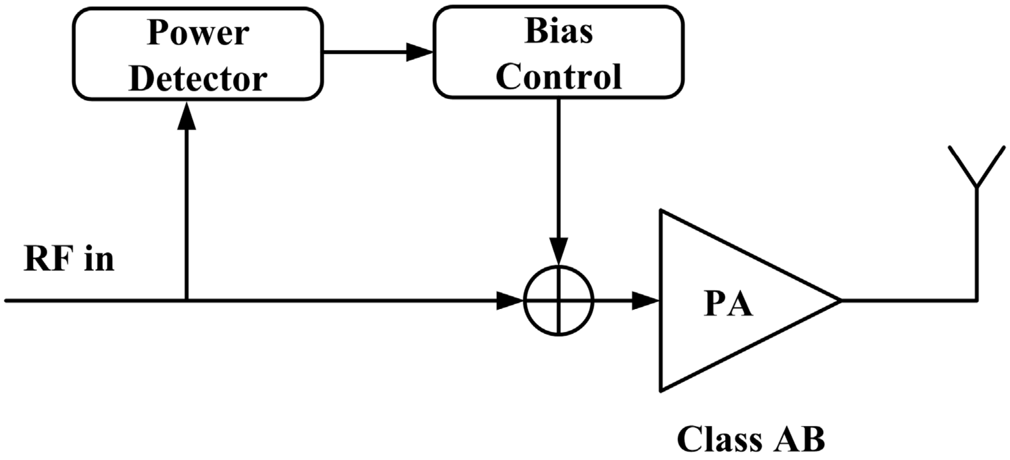
$$\eta_2 = \frac{V_p^2/(2R_{in})}{(V_p/R_{in})V_{DD}} = \frac{V_p}{2V_{DD}}.$$

- If in addition the supply voltage scales, the drain efficiency remains constant at 50%



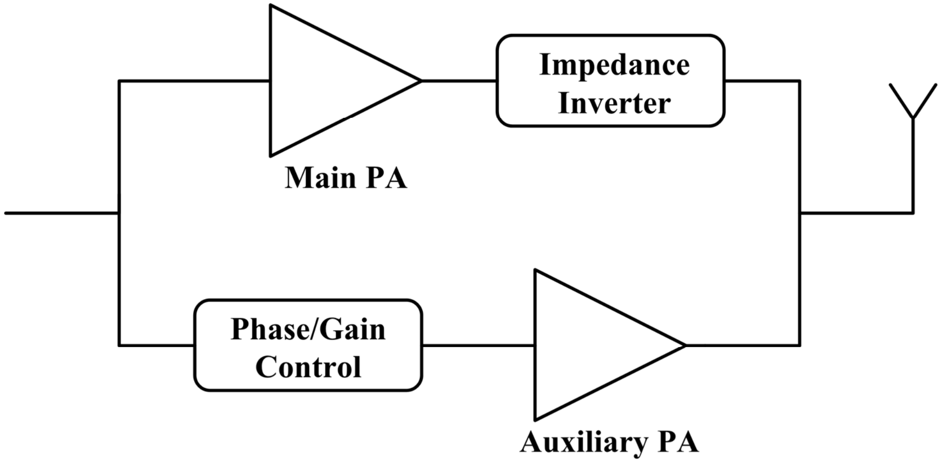
Envelope Tracking

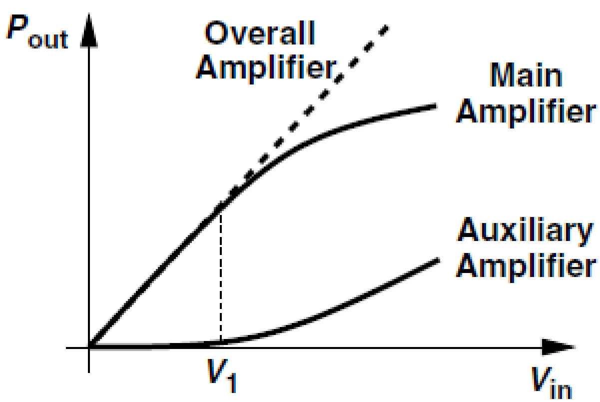
- Envelope tracking amplifiers dynamically adjust the bias point of the main PA to improve efficiency at power back-off
- One way to implement such a transmitter is to add a power detector (or an envelope detector) in the RF path
- The power detector provides information on output power and dynamically adjusts the bias point of the PA (supply voltage or bias current)
- Envelope tracking does not improve peak efficiency, only average



Doherty Amplifier

- Doherty amplifier uses two amplifiers to improve the overall linearity while achieving better efficiency
- The main PA usually operates in class A or AB
- In the high output power regime this amplifier starts to saturate effectively loosing its linearity
- At that point the auxiliary amplifier (usually class C) kicks in to compensate for the nonlinearity of the main amplifier



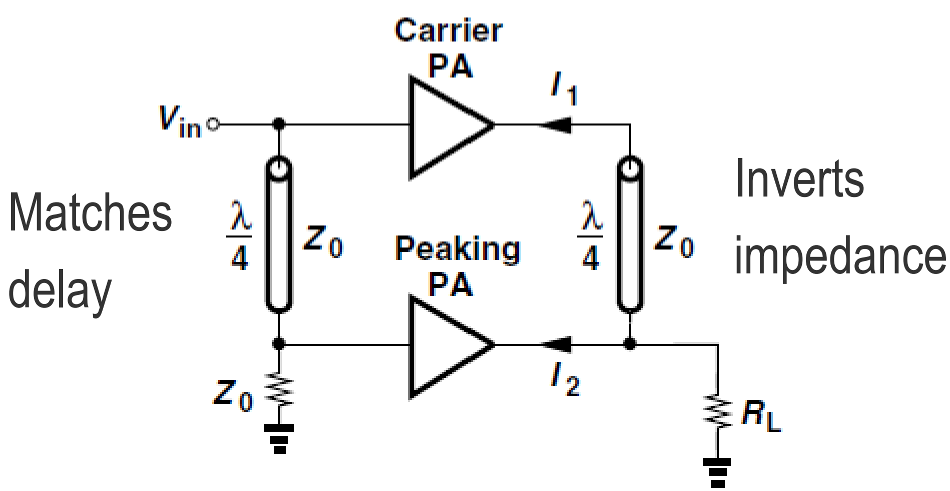


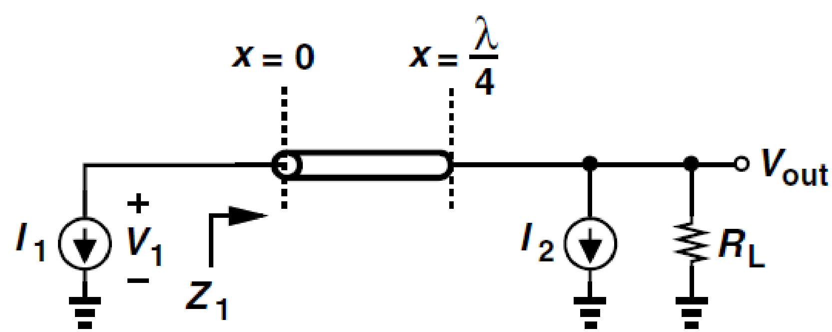
Doherty Amplifier

- The problem is how to tie the two amplifiers
- The transmission line at the output of the main (carrier) PA inverts the impedance
- It can be shown that the impedance of the main amplifier is a function of the relative strengths of the two amplifiers α

$$Z_1 = Z_0 \left(\frac{Z_0}{R_L} - \alpha \right)$$

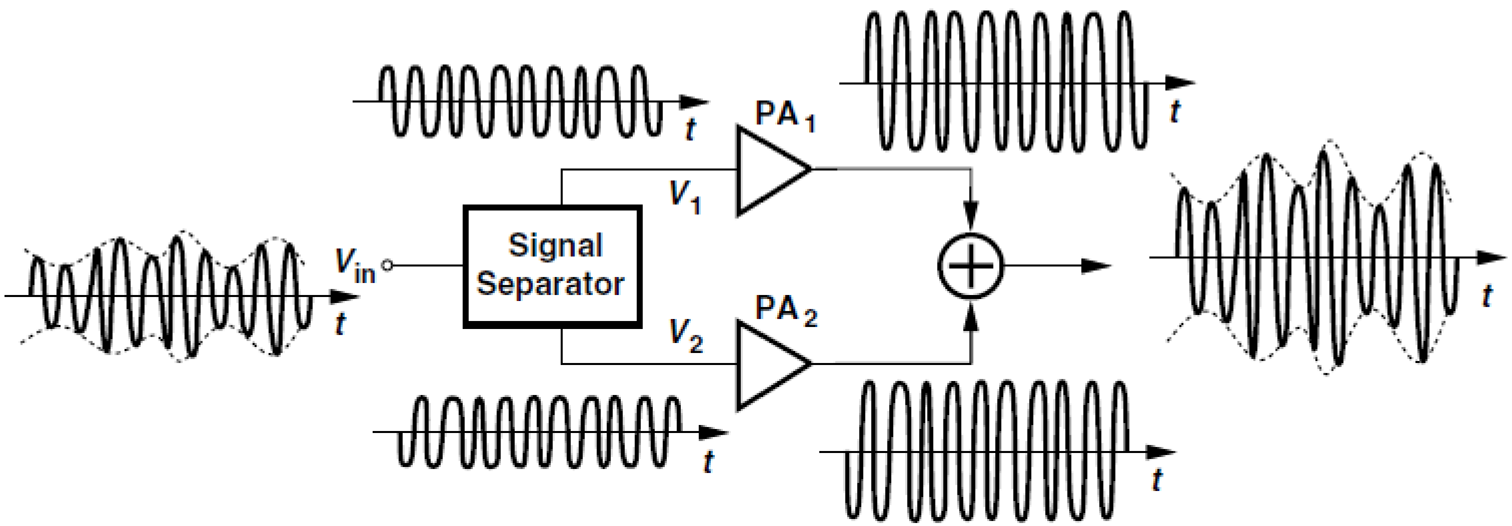
- As the output power increases so does α, maintaining constant drain voltage of the main amplifier as the power increases (load modulation)





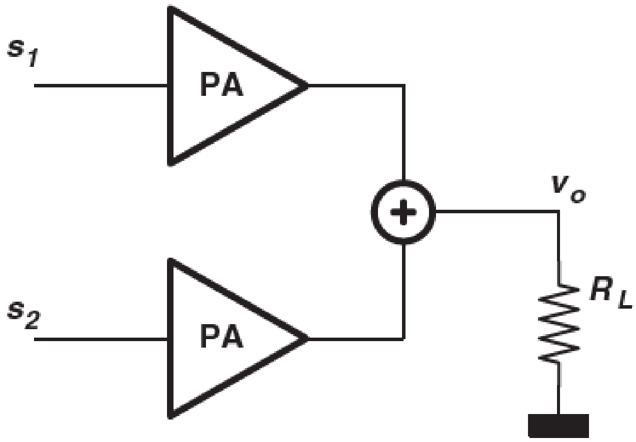
Outphasing

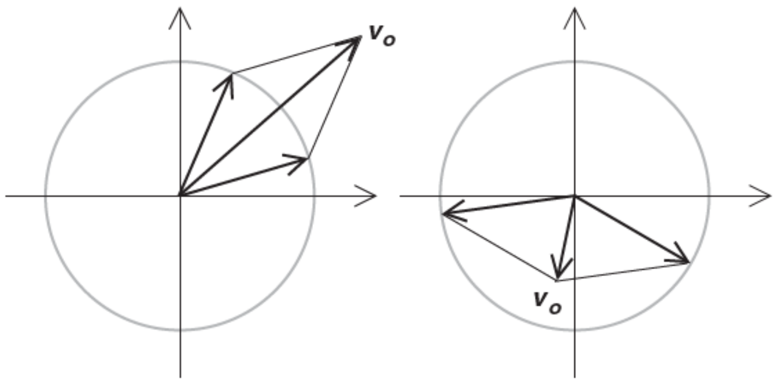
- Basic idea: use two constant envelope amplifiers to produce a non-constant envelope signal (also known as LINC - LInear amplification with Nonlinear Components)
- By varying the phase of V1 and V2 a variable envelope signal can be generated
- Since the two PAs can be nonlinear a high efficiency can be achieved



Outphasing

- It is easy to see how to generate the two outphasing signals by looking at the phasor diagram
- The two signals can be generated in the baseband and then upconverted to the carrier frequency (more efficient than separating the two phase modulated signals at RF)
- The main issue is how to implement an efficient combiner for the two signals



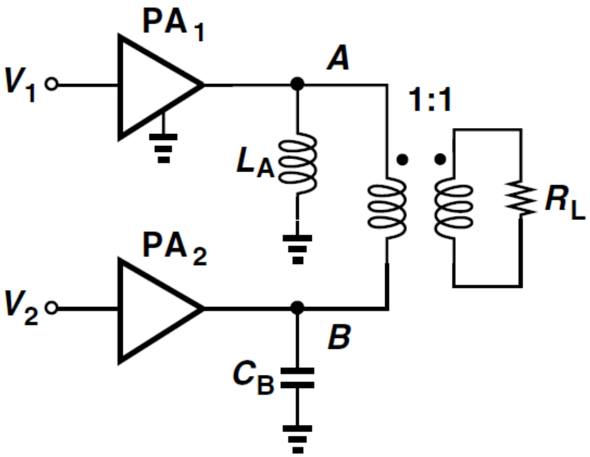


Outphasing

- Issues with outphasing:
- Mismatch between the two paths
- Larger bandwidth needed for the two outphasing signals than the composite signal
- Interaction between the two amplifiers through the combining network
  - Ideal combiner should be passive, lossless and provide perfect isolation
  - In reality the signal of one amplifier affects the other
  - Assuming the two amplifiers act as voltage buffers and that an ideal transformer is used for summation it can be shown that impedances seen by each amplifier are given by:

$$Z_1 = \frac{R_L}{2} - j\cot\theta\frac{R_L}{2}$$

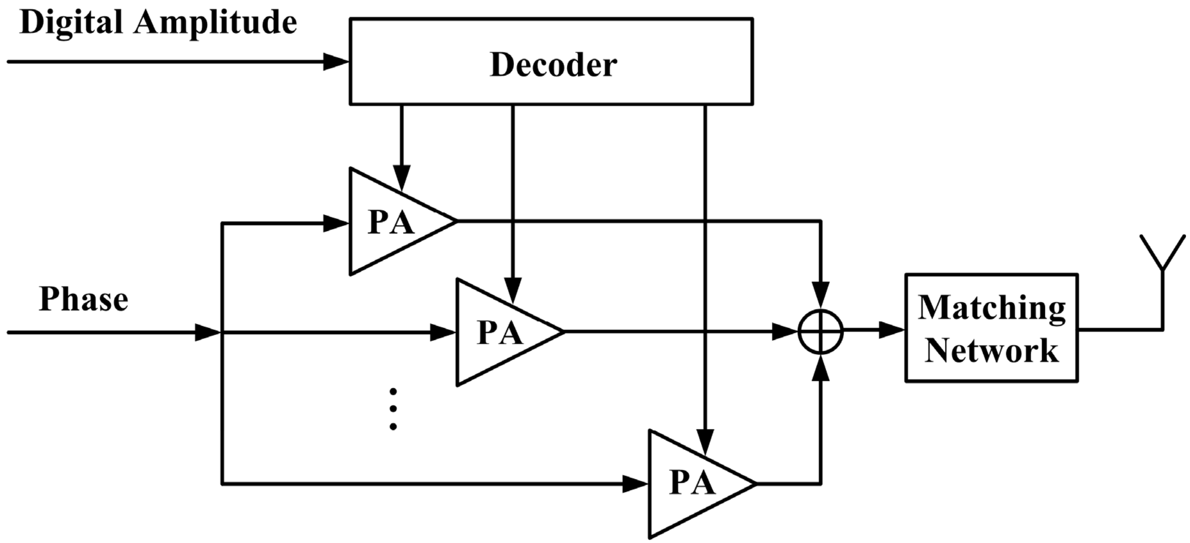
$$Z_2 = \frac{R_L}{2} + j\cot\theta\frac{R_L}{2}.$$



  - Can be partially negated by parallel reactances
  - Chireix's combiner

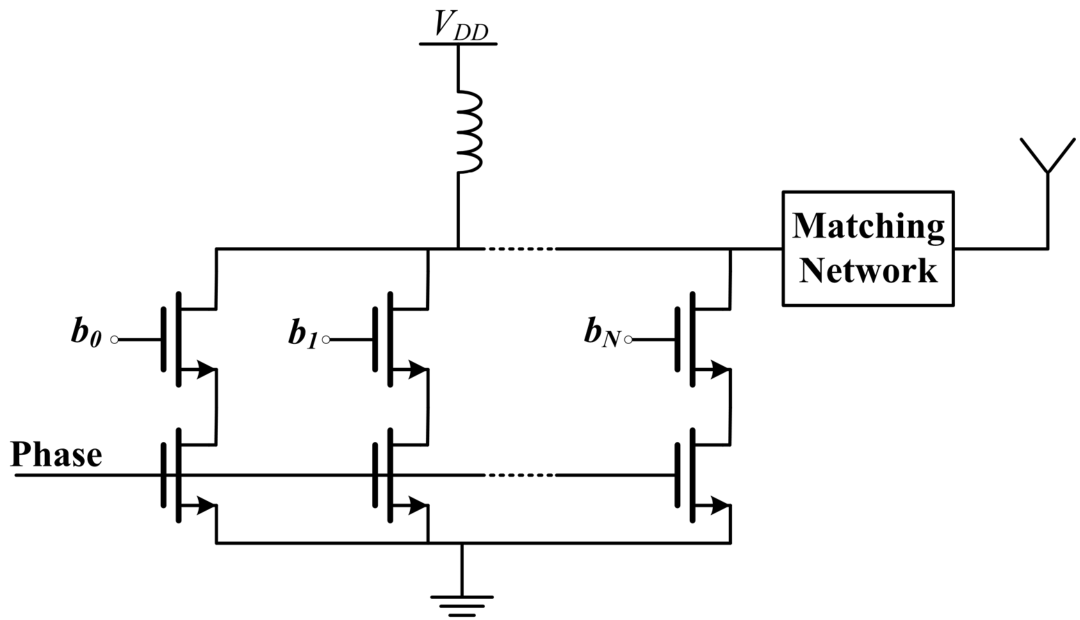
Digitally Controlled PA

- Quadrature baseband signals can be converted to amplitude and phase signals in the baseband
- Phase signal is then directly used to control the frequency synthesizer
- Amplitude signal (digital) can be used to control the output power
- In this example the PA is split into slices, each slice driven by the same phase modulated carrier
- Different stages can be turned on and off to control output power



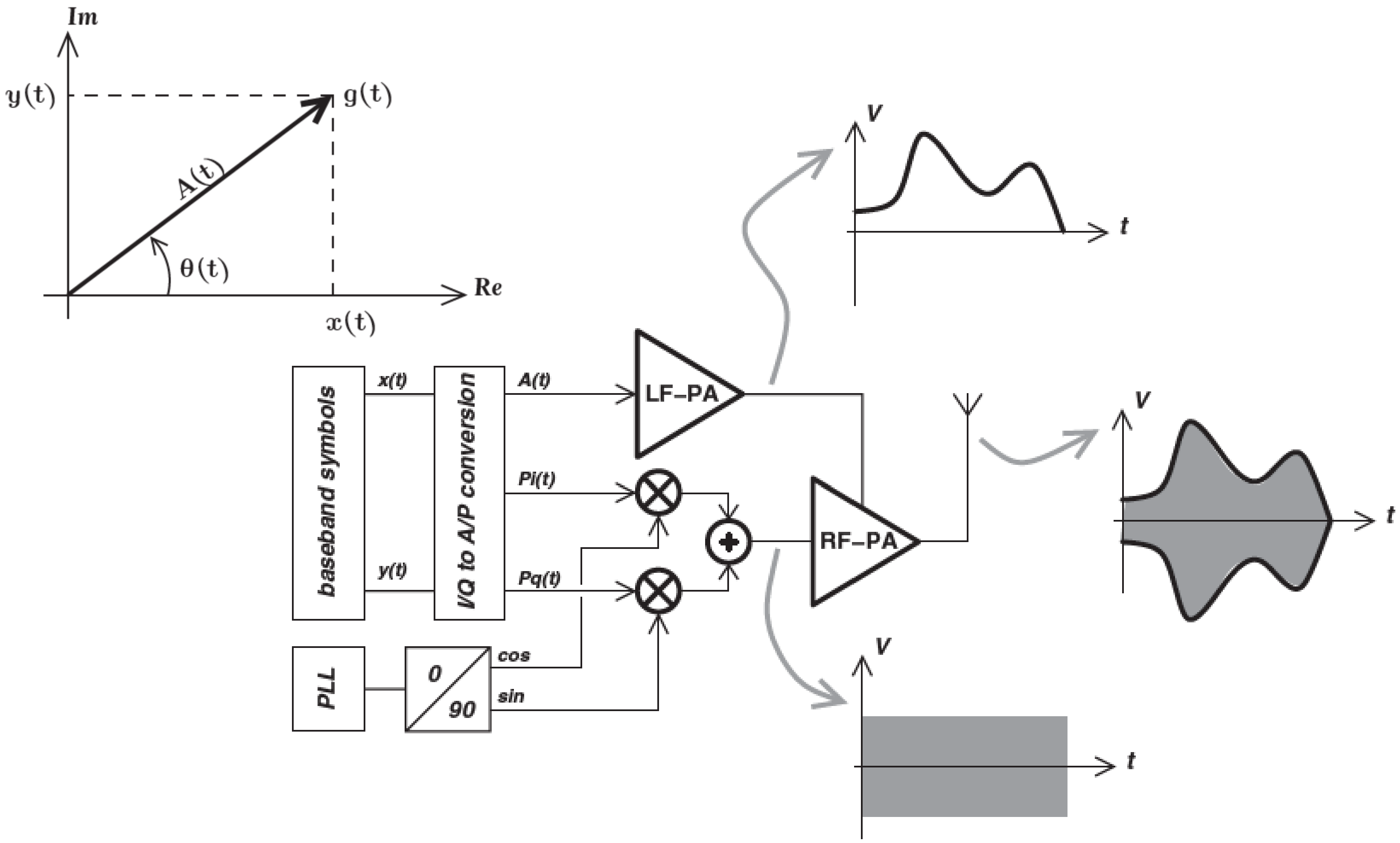
Digitally Controlled PA

- One way to implement digital control is to simply turn the cascode transistor on and off
- No combining network - all PA slices must operate as current sources to sum the currents at the output
- Similar to controlling the bias point of the PA
- Moderate efficiency combined with good linearity



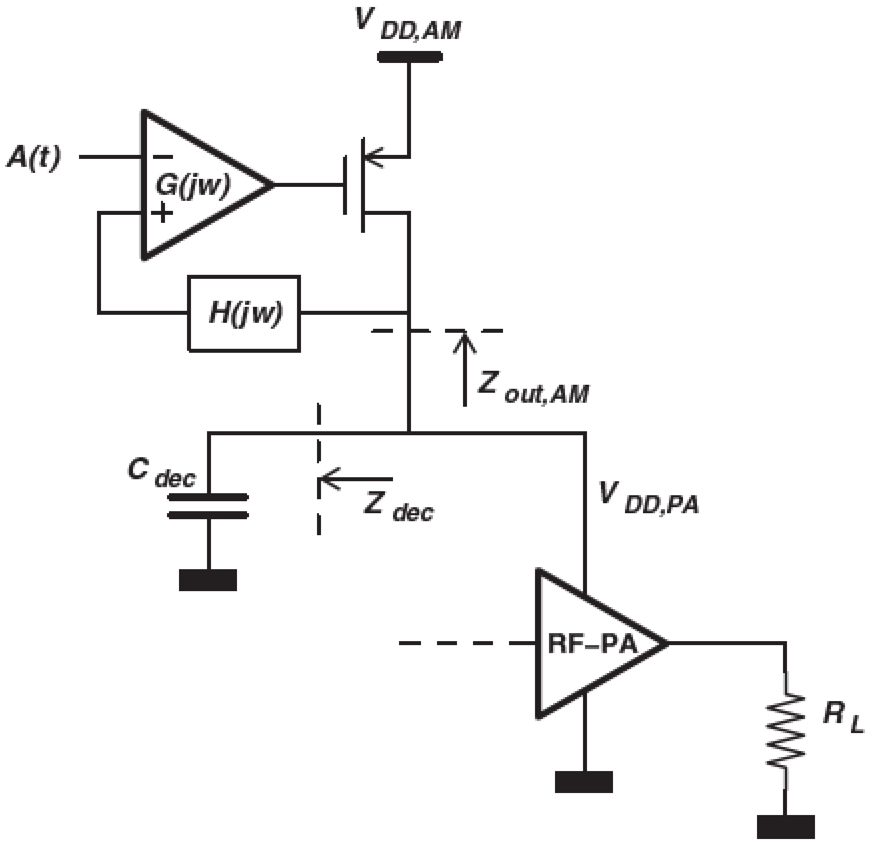
Polar Amplifiers

- Polar amplifiers use amplitude and phase signals instead of I and Q signals



Polar Amplifiers

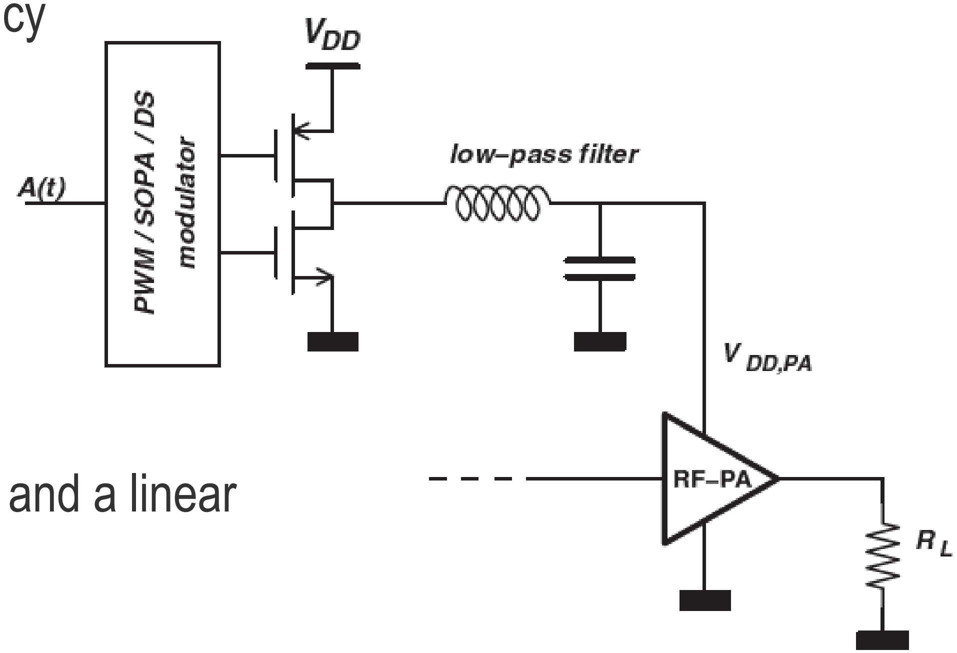
- In the previous example a digital signal controls a number of linear Pas
- Now, instead of using a large number of linear PAs, the idea is to find a way to control output power of the class E PA
- Need hard switching at the input, output power cannot be controlled using the input signal
- Output power of a class E stage determined by the supply voltage
- It is possible to use voltage regulator to modulate the supply of the class E power amplifier



Polar Amplifiers

- Loss in the linear regulator limits achievable efficiency
- The lower the supply voltage the more power is lost in the regulator
- It is possible to use a switching regulator instead
- Capable of achieving very high efficiency
- Issues:
- Ripple coupled to output
- Bandwidth of the amplitude signal
- Stability of the converter
- One solution is to combine a switching and a linear

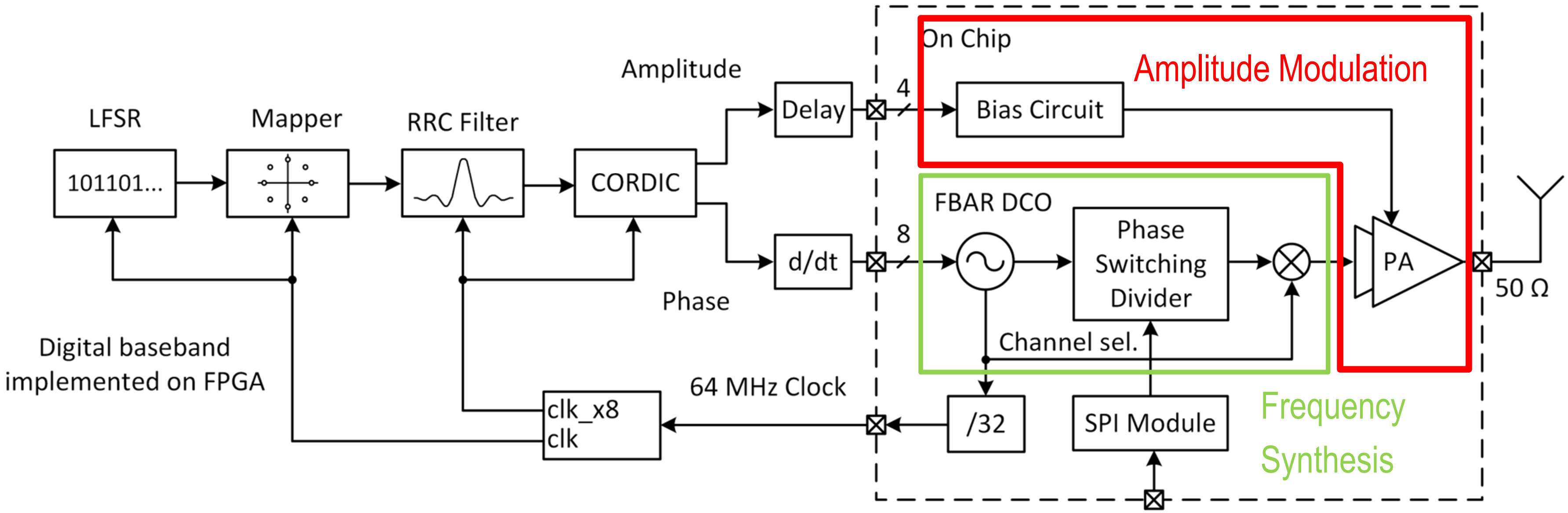
Regulator to get the best of both



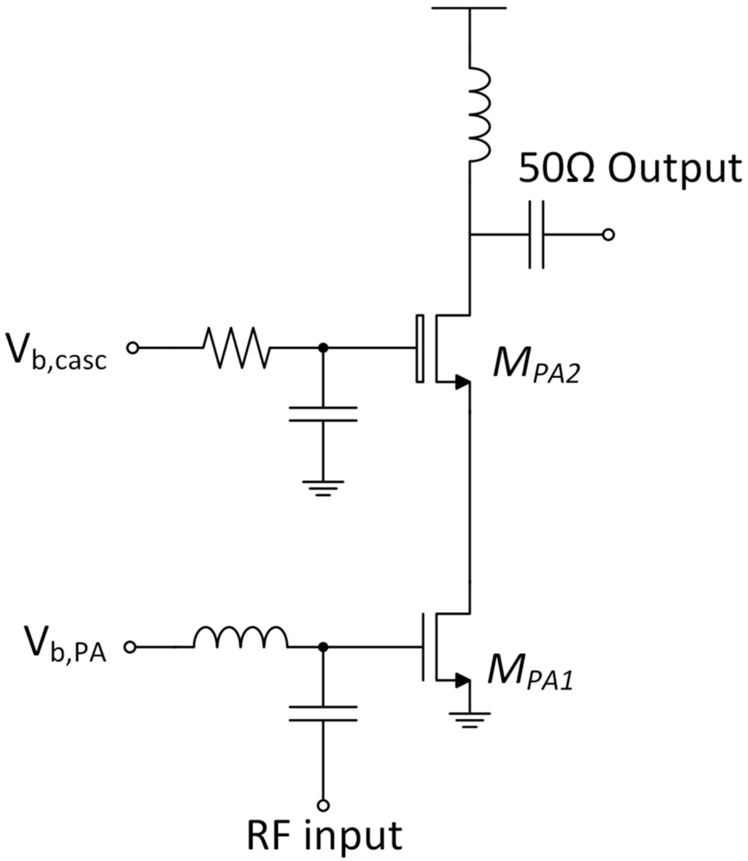
Polar Amplifiers

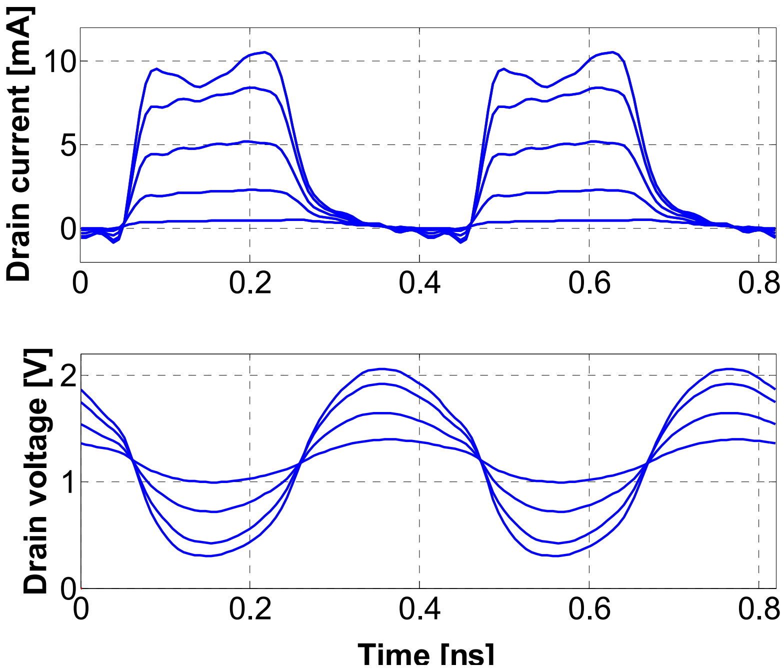
- Problems with the polar architecture
- Delay mismatch between the amplitude and phase path
  - Causes spectral regrowth
  - May require complex compensation techniques if high linearity is required
- AM-PM conversion
  - Changes in amplitude affect the phase of the output signal
  - Again results in spectral regrowth

Example Polar Amplifier

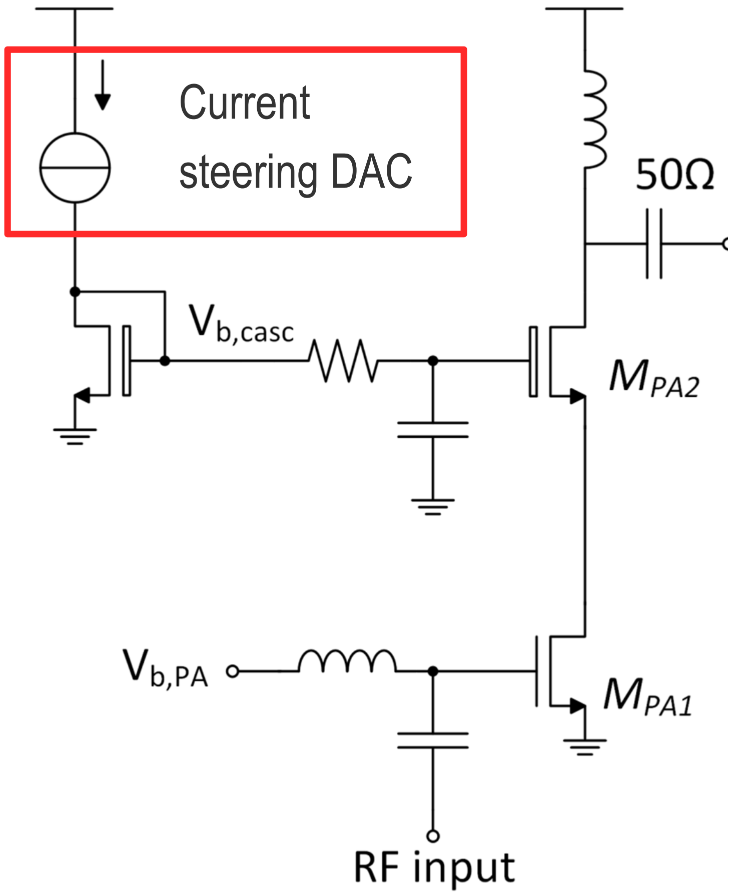


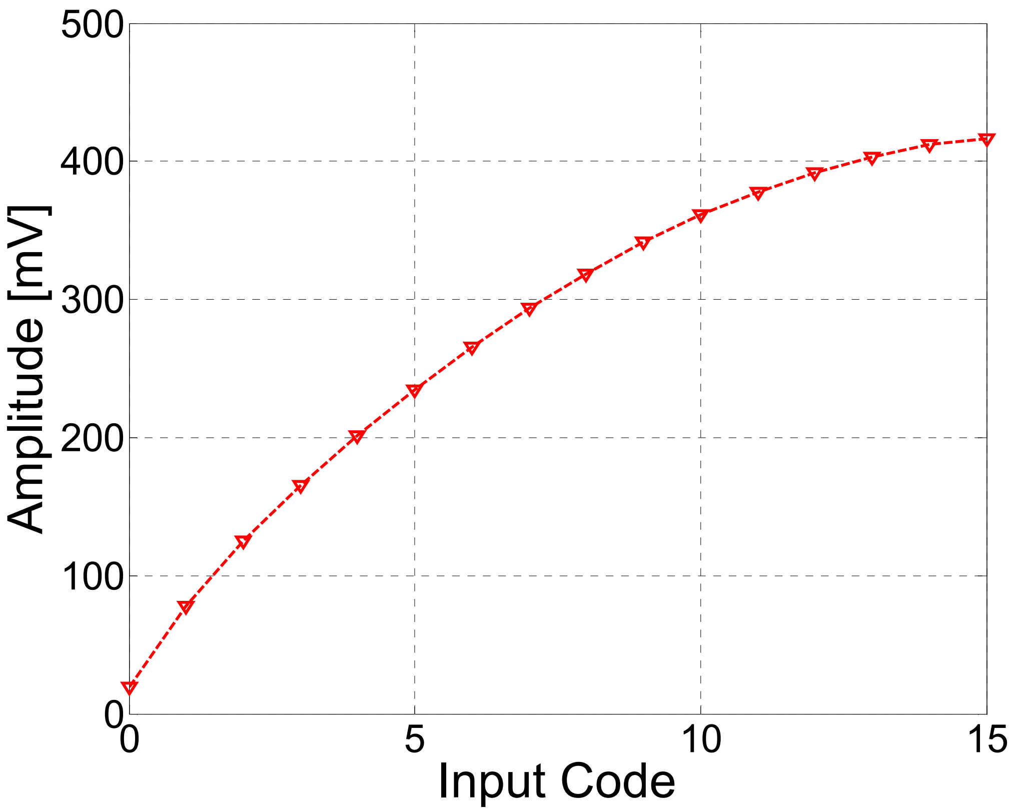
Example Polar Amplifier



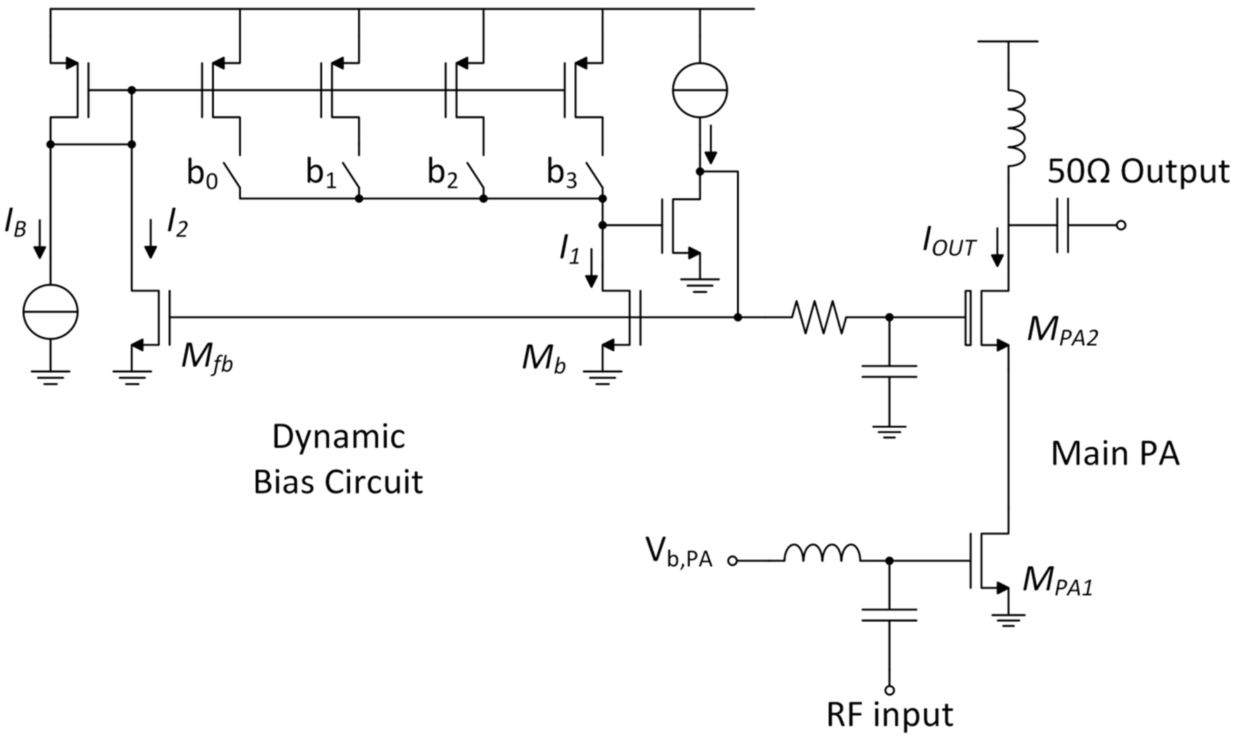


Example Polar Amplifier

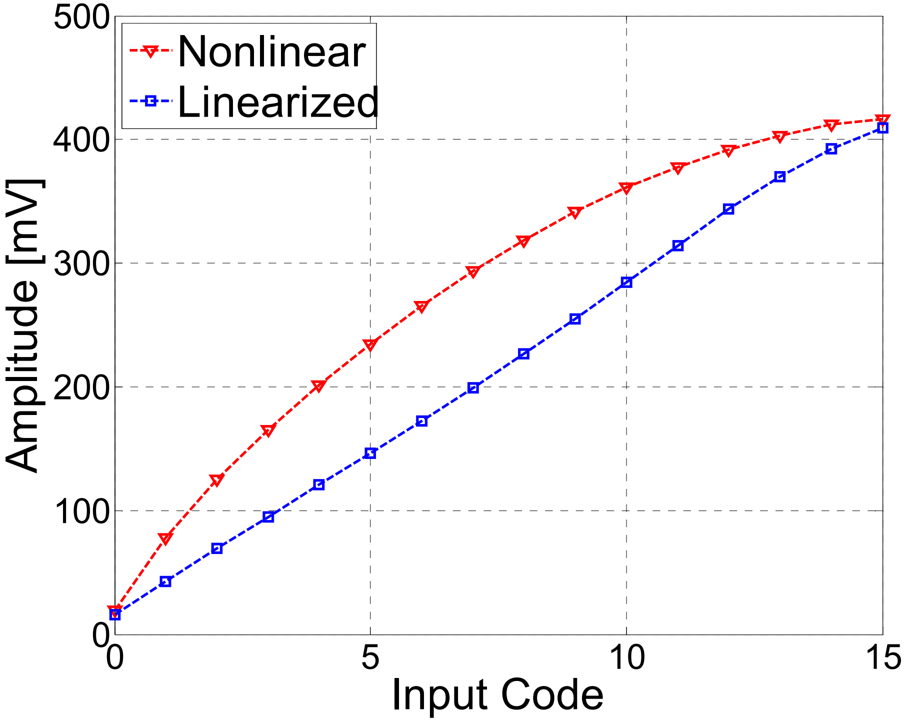


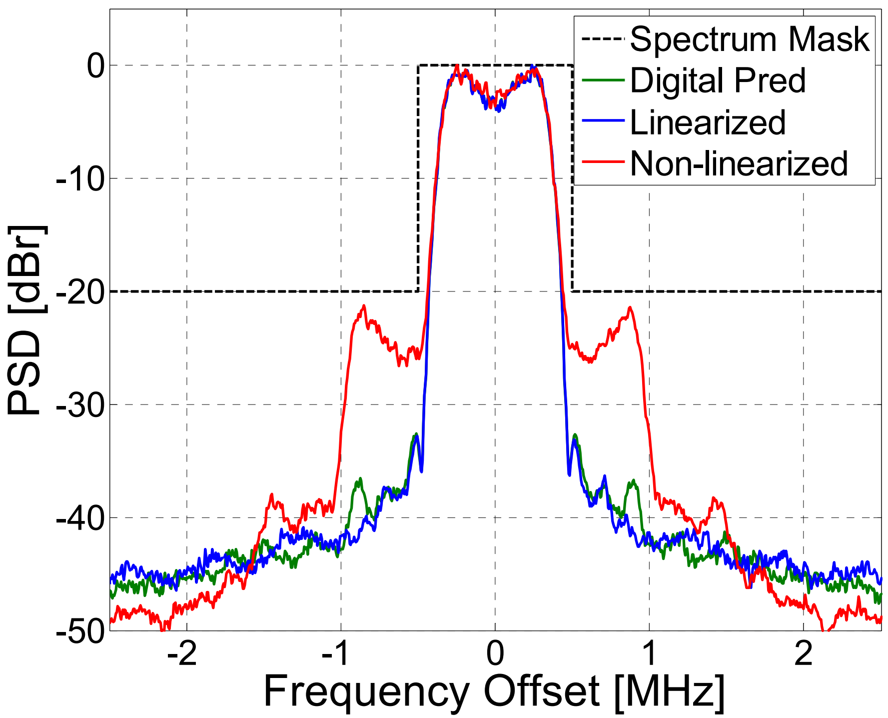


Example Polar Amplifier



Example Polar Amplifier





Example Polar Amplifier