MICRO-461
Low-power Radio Design for the IoT

8. Low Noise Amplifiers (LNAs)

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Outline

- **Low-Noise Amplifiers**
- Low-power LNA Design

General Considerations

- Since the LNA is the 1st-gain stage in the Rx path, its NF directly adds to the system NF
- The typical Rx noise figure ranges from 6 to 8 dB, it is expected that the antenna switch or duplexer contributes about 0.5 to 1.5 dB, the LNA about 2 to 3 dB, and the remainder of the chain about 2.5 to 3.5 dB
- The equivalent noise PSD at the input is given by $S_{neq} = 4kTR_{neq}$, the NF of a common-source LNA (neglecting the induced gate noise and the contributions of the following stages) is then simply

$$F = \frac{R_{neq}}{R_S} \cong 1 + \frac{\gamma_{nD}}{G_m \cdot R_S}$$

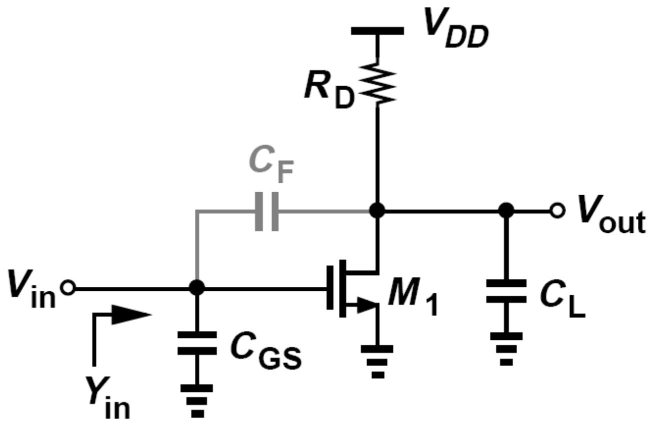
- Assuming the MOST is biased in strong inversion $G_m = 2I_D/(V_G - V_{T0})$
- With $NF = 2dB$ and $R_S = 50\Omega$, $R_{Neq} = 29\Omega$. Neglecting the induced gate noise and assuming $V_G - V_{T0} = 400mV$ the bias current is then 4.5 mA

General Considerations

- In addition to noise requirements, the LNA should also offer sufficient gain in order to reduce the noise contribution of the following stages
- It should have a sufficiently high IIP3 to avoid any intermodulation at the input
- Most of the time a 50Ω input (sometimes also output) impedance is (are) required
- The return input (output) loss should be small, the reverse isolation should be large and the LNA should be stable

Input Matching – Common Source Amplifier

- Several circuit configurations can be used to create a 50Ω input resistance



$$G_{in} = \Re\{Y_{in}\} = \omega^2 R_D C_F \frac{C_F + G_m R_D (C_L + C_F)}{1 + \omega^2 R_D^2 (C_L + C_F)^2}$$

$$B_{in} = \Im\{Y_{in}\} = \omega C_F \frac{1 + G_m R_D + \omega^2 R_D^2 C_L (C_L + C_F)}{1 + \omega^2 R_D^2 (C_L + C_F)^2}$$

- Assuming $G_m R_D \gg 1$, $C_L \gg C_F$ and $\omega \approx 1/(R_D C_L)$

$$G_{in} = \Re\{Y_{in}\} \cong \frac{G_m}{2} \frac{C_F}{C_L}$$

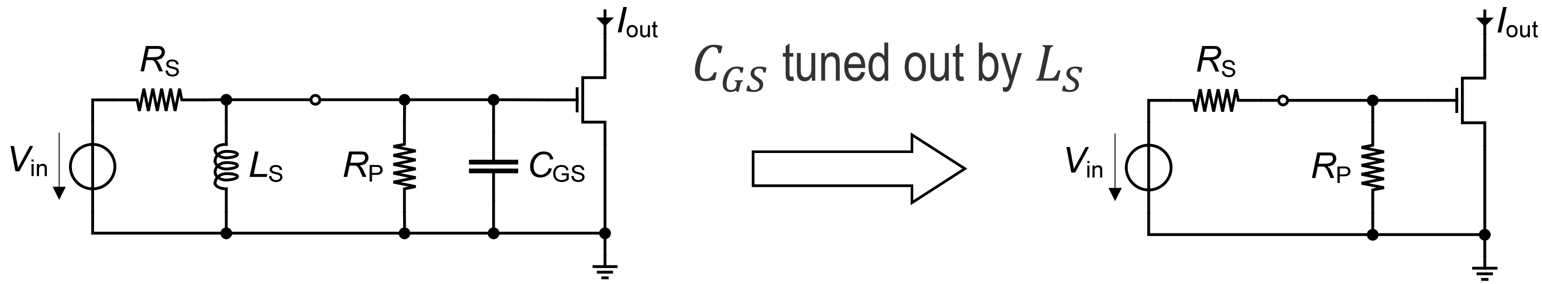
$$B_{in} = \Im\{Y_{in}\} \cong \omega C_F \frac{G_m R_D}{2}$$

- Proper choice of $2C_L/(G_m C_F)$ can yield 50Ω input resistance
- Low voltage gain at high frequencies due to bandwidth limitation at the output node

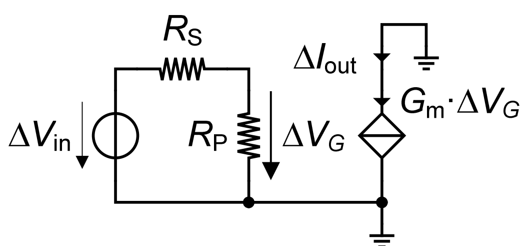
Common Source LNA (without matching network-LNA1)

- A resistor R_P can be added in parallel with the input and capacitance C_{GS} can be tuned out with an external inductor

at resonance frequency



- The equivalent transconductance (at resonance frequency) can be calculated from

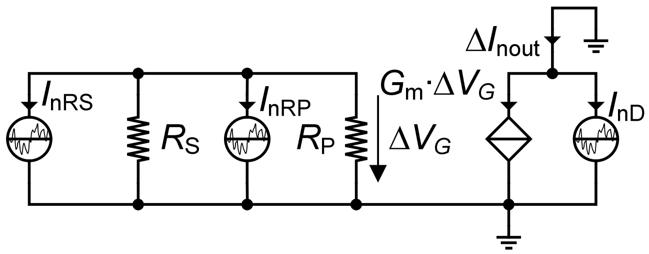


$$G_{meq} = \frac{R_P}{R_S + R_P} \cdot G_m = \frac{G_m}{2} \quad \text{for} \quad R_P = R_S$$

A.-S. Porret, PhD Thesis, No. 2542, EPFL, 2002.

Common Source LNA (without matching network-LNA1)

- The thermal noise at the output (at resonance frequency) is given by



$$G_{nout} = G_{nD} + \left(G_m \frac{R_S R_P}{R_S + R_P} \right)^2 \left(\frac{1}{R_S} + \frac{1}{R_P} \right)$$

- The input-referred equivalent noise resistance (including R_S noise) is given by

$$R_{neq} = \frac{G_{nout}}{G_{meq}^2} = R_S + \frac{R_S^2}{R_P} + \left(1 + \frac{R_S}{R_P}\right)^2 \frac{G_{nD}}{G_m^2} = R_S + \frac{R_S^2}{R_P} + \left(1 + \frac{R_S}{R_P}\right)^2 \frac{\gamma_{nD}}{G_m}$$

- Finally the noise factor is obtained as

$$F = \frac{R_{neq}}{R_S} = 1 + \frac{R_S}{R_P} + \left(1 + \frac{R_S}{R_P}\right)^2 \frac{\gamma_{nD}}{G_m R_S} = 2 + \frac{4\gamma_{nD}}{G_m R_S} \quad \text{for} \quad R_P = R_S$$

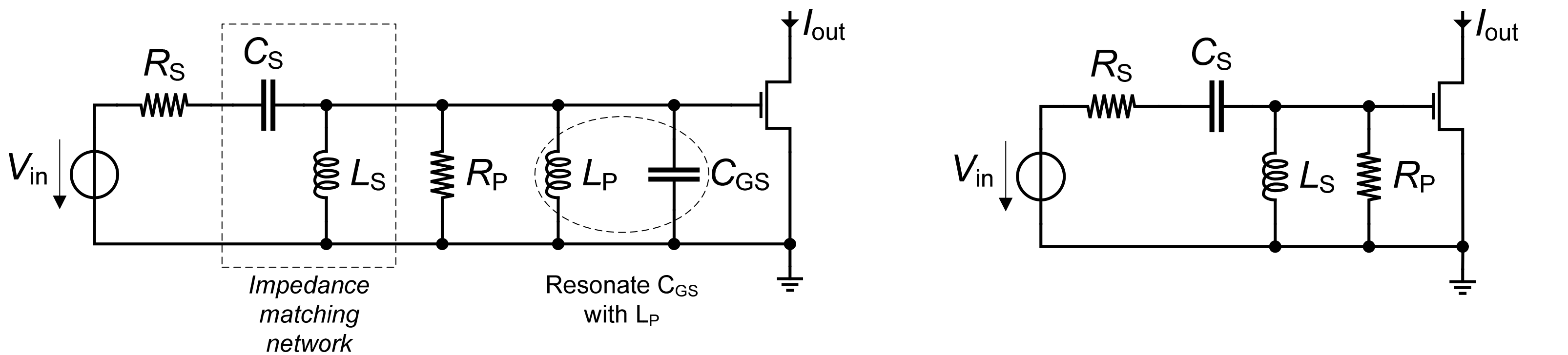
- Termination resistance R_P **adds noise** and **lowers the gain by 6dB**
- CS amplifier without termination R_P ($R_P \to \infty$ in above expression)

$$F = 1 + \frac{\gamma_{nD}}{G_m R_S}$$

📖 A.-S. Porret, PhD Thesis, No. 2542, EPFL, 2002.

Common Source LNA (with matching network-LNA2)

- Resistance R_P can be made larger to reduce its noise current contribution
- An impedance matching network has then to be added in order to reduce the impedance seen from the source so it matches the source resistance



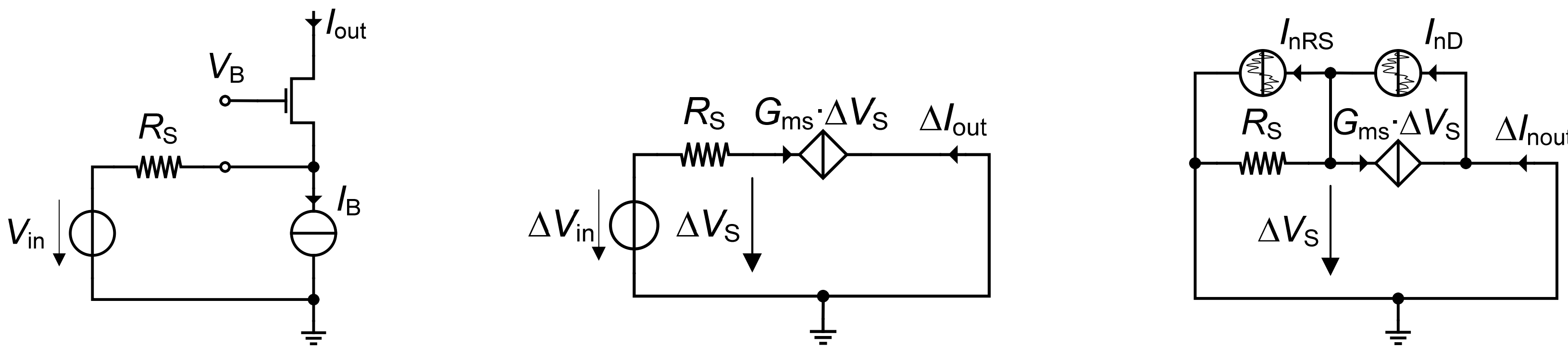
$$Q = \frac{X_S}{R_S} = \frac{R_P}{X_P} = \sqrt{\frac{R_P}{R_S} - 1} \qquad X_P = \omega_0 L_S = \frac{R_P}{Q} \qquad X_S = \frac{1}{\omega_0 C_S} = Q R_S \qquad R_P = \left(1 + Q^2\right) R_S$$

- Voltage gain, equivalent transconductance and noise factor are then given by

$$A_v = \frac{\Delta V_G}{\Delta V_S} = \frac{1 + jQ}{2} \qquad G_{meq} \triangleq \frac{\Delta I_{out}}{\Delta V_{in}} = A_v G_m = \left(1 + jQ\right) \frac{G_m}{2} \qquad F = 2 + \frac{4 \gamma_{nD}}{\left(1 + Q^2\right) G_m R_S}$$

A.-S. Porret, PhD Thesis, No. 2542, EPFL, 2002.

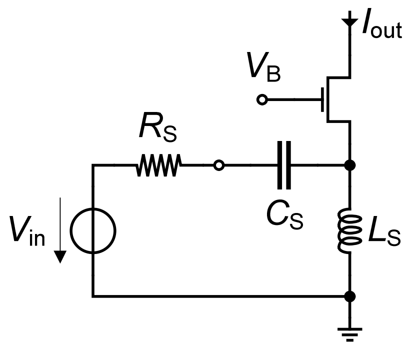
Common Gate LNA (without matching network-LNA3)

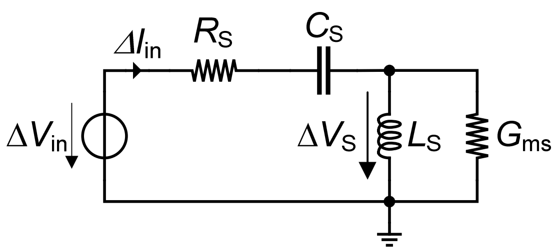


- Input impedance: $$Z_{in} = \frac{1}{G_{ms}}$$
- Equivalent transconductance: $$G_{meq} = \frac{\Delta I_{out}}{\Delta V_{in}} = -\frac{G_{ms}}{1+G_{ms}R_S}\bigg|_{G_{ms}R_S=1} = -\frac{G_{ms}}{2}$$
- Input-referred noise resistance: $$R_{neq} = R_S + \frac{G_{nD}}{G_{ms}^2} = R_S + \frac{\delta_{nD}}{G_{ms}}$$
- Noise factor: $$F = \frac{R_{neq}}{R_S} = 1 + \frac{\delta_{nD}}{G_{ms}R_S}\bigg|_{G_{ms}R_S=1} = 1+\delta_{nD}$$

A.-S. Porret, PhD Thesis, No. 2542, EPFL, 2002.

Common Gate LNA (with matching network-LNA4)





- If R_S is too small it will lead to a high value of G_{ms} for having $Z_{in} = 1/G_{ms} = R_S$, which results in a high power consumption
- An input impedance matching network is required, with the following parameters:

$$Q = \frac{X_S}{R_S} = \frac{R_P}{X_P} = \sqrt{\frac{R_P}{R_S} - 1} \qquad X_P = \omega_0 L_S = \frac{1}{Q G_{ms}} \qquad X_S = \frac{1}{\omega_0 C_S} = Q R_S$$

- The real part of the input impedance is then given by

$$R_{in} \triangleq \Re\{Z_{in}\} = \frac{1}{G_{ms}\left(1+Q^2\right)}$$

- Input matching is then obtained by setting $R_{in} = R_S$, which leads to

$$G_{ms} = \frac{1}{\left(1+Q^2\right) R_S} \quad \text{for which} \quad R_{in} = R_S \quad \text{and} \quad X_{in} \triangleq \Im\{Z_{in}\} = 0$$

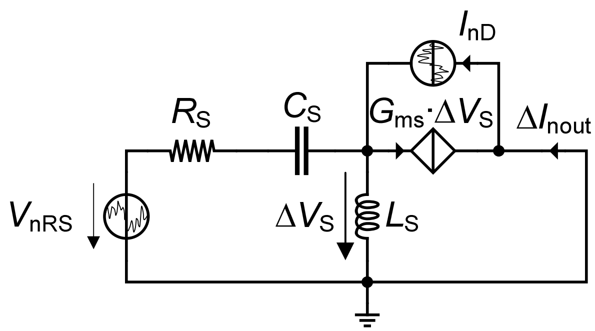
Common Gate LNA (with matching network-LNA4)

- The voltage gain from ΔV_{in} to ΔV_S under impedance matching is given by

$$A_v = \left.\frac{\Delta V_S}{\Delta V_{in}}\right|_{\text{matched}} = \frac{1+jQ}{2}$$

- Which leads to an equivalent transconductance given by

$$G_{meq}\Big|_{\text{matched}} = \left.\frac{\Delta I_{out}}{\Delta V_{in}}\right|_{\text{matched}} = A_v \cdot G_{ms} = (1+jQ)\cdot\frac{G_{ms}}{2}$$



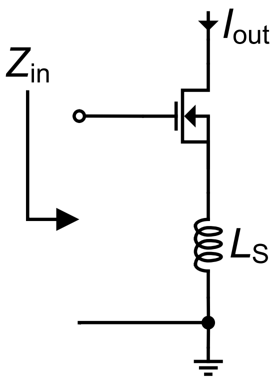
- The total input noise resistance and noise factor under the above matched condition are then given by

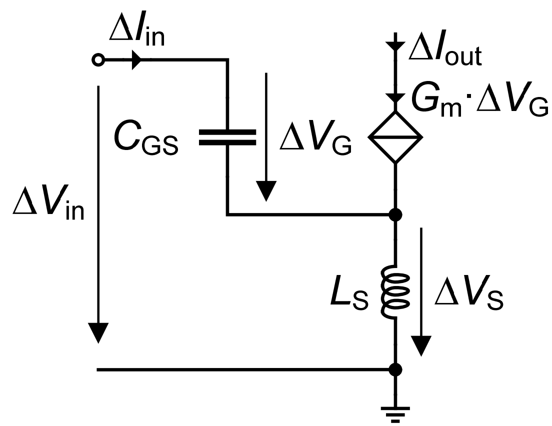
$$R_{neq}\Big|_{\text{matched}} = R_S + R_S\delta_{nD} \qquad F\Big|_{\text{matched}} = \frac{R_{neq}}{R_S} = 1+\delta_{nD}$$

📖 A.-S. Porret, PhD Thesis, No. 2542, EPFL, 2002.

Common Source Inductively Degenerated LNA (LNA5)

- Another method of creating a resistive input impedance without degrading the noise performance is to use inductive source degeneration



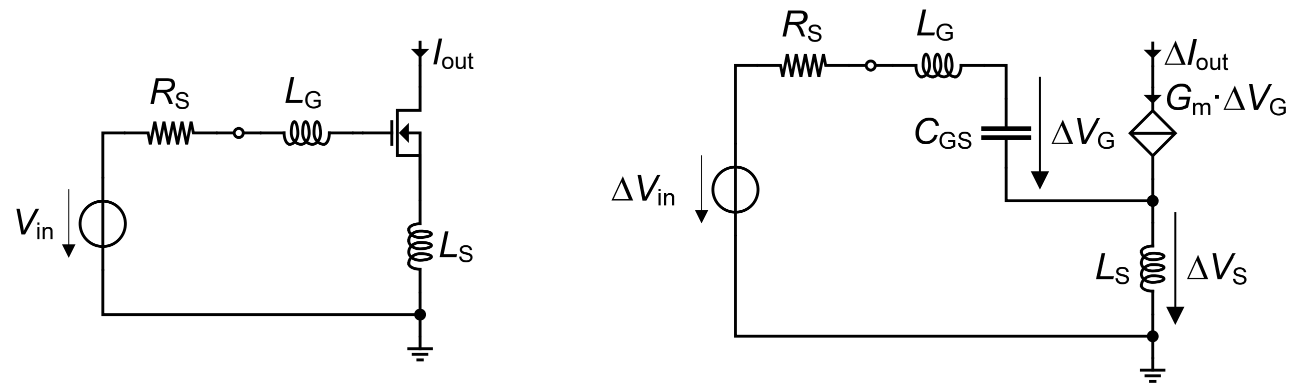


$$Z_{in} = \frac{G_m L_S}{C_{GS}} + sL_S + \frac{1}{sC_{GS}}$$

$$Z_{in} = \frac{G_m L_S}{C_{GS}} + j\frac{\omega^2 L_S C_{GS} - 1}{\omega C_{GS}}$$

- Z_{in} purely resistive at the resonant frequency set by C_{GS} and L_S
- However, L_S is actually chosen to match the source resistance R_S and hence cannot be used to tune out C_{GS}
- Additional degree of freedom is required to eliminate the remaining imaginary part
- Can be done by adding a series inductor L_G at the gate

Common Source Inductively Degenerated LNA (LNA5)



- The remaining imaginary part can be tuned out thanks to a series inductor L_G
- The voltage gain from the input to the gate is then given by

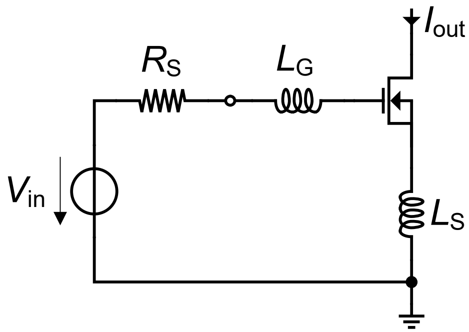
$$A_v = \frac{\Delta V_G}{\Delta V_{in}} = \frac{1}{1+(G_m L_S + R_S C_{GS})s + (L_G + L_S) C_{GS} s^2} = \frac{1}{1+\dfrac{s}{\omega_0 Q}+\left(\dfrac{s}{\omega_0}\right)^2}$$

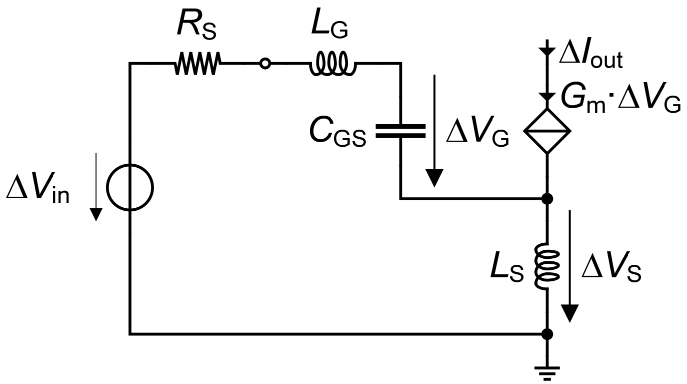
with $\omega_0 = \dfrac{1}{\sqrt{(L_G + L_S) C_{GS}}}$ and $Q = \dfrac{1}{(G_m L_S + R_S C_{GS})\omega_0}$

- The maximum voltage is reached for $\omega = \omega_0$ and is simply equal to Q

$$A_{v\max} = A_v(\omega = \omega_0) = Q = \frac{1}{(G_m L_S + R_S C_{GS})\omega_0} = \frac{1}{G_m \omega_0 L_S + 1/Q_L} \quad \text{with} \quad Q_L = \frac{1}{R_S \omega_0 C_{GS}}$$

Common Source Inductively Degenerated LNA (LNA5)





- The equivalent transconductance $G_{meq} \triangleq \Delta I_{out}/\Delta V_{in}$ at resonance is now boosted by the Q of the series resonant circuit

$$G_{meq0} = G_{meq}(\omega = \omega_0) = A_{v\max} G_m = \frac{G_m}{(G_m L_S + R_S C_{GS})\omega_0}$$

- The input impedance is then given by

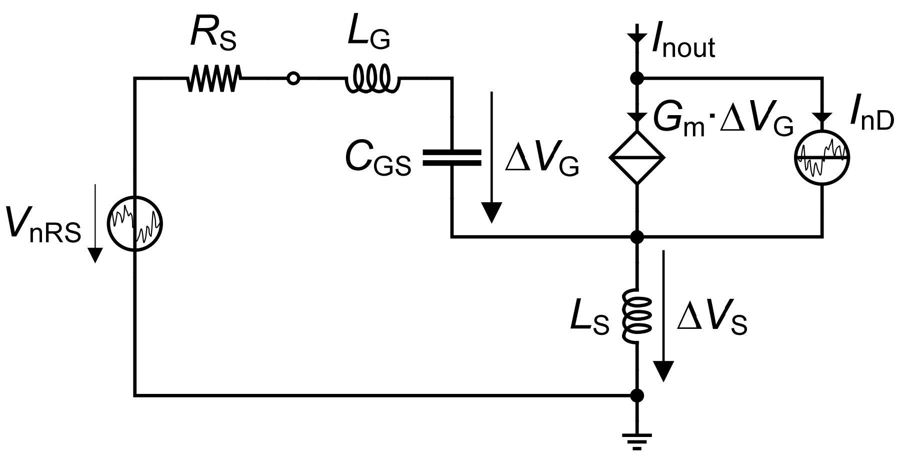
$$Z_{in} = \frac{G_m L_S}{C_{GS}} + s(L_S + L_G) + \frac{1}{sC_{GS}} \qquad Z_{in} = \frac{G_m L_S}{C_{GS}} + j\frac{\omega^2 (L_S + L_G) C_{GS} - 1}{\omega C_{GS}} \qquad Z_{in}\big|_{\omega=\omega_0} = \frac{G_m L_S}{C_{GS}}$$

- For impedance matching $R_S = G_m L_S / C_{GS}$ and hence

$$G_m L_S = R_S C_{GS} \quad \Rightarrow \quad G_{meq0} = \frac{G_m}{2 R_S C_{GS} \omega_0} = \frac{\omega_t}{2 R_S \omega_0} \quad \text{with} \quad \omega_t \cong \frac{G_m}{C_{GS}}$$

Common Source Inductively Degenerated LNA (LNA5)

- The noise factor F at $\omega = \omega_0$ is then calculated from the circuit below



$$I_{nout} = G_{meq} V_{nRS} + \left(1 - G_{meq} s L_S\right) I_{nD}$$

$$V_{neq} = \frac{I_{nout}}{G_{meq}} = V_{nRS} + \left(\frac{1}{G_{meq}} - s L_S\right) I_{nD}$$

$$= V_{nRS} + \frac{1 + R_S C_{GS} s + (L_G + L_S) C_{GS} s^2}{G_m} I_{nD}$$

$$V_{neq}(\omega_0) = V_{nRS} + j \frac{R_S C_{GS} \omega_0}{G_m} I_{nD}$$

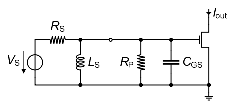
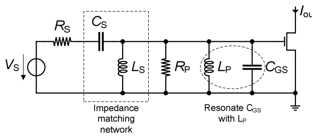
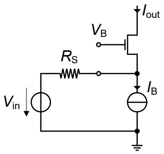
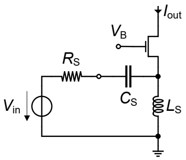
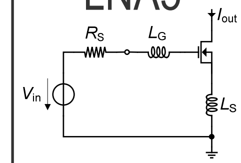
- From which we get the input referred noise resistance R_{neq}

$$R_{neq}(\omega_0) = R_S + \left(\frac{R_S C_{GS} \omega_0}{G_m}\right)^2 \cdot G_{nD} = R_S + \left(\frac{R_S C_{GS} \omega_0}{G_m}\right)^2 \cdot \gamma_{nD} G_m = R_S + \frac{\left(R_S C_{GS} \omega_0\right)^2 \gamma_{nD}}{G_m}$$

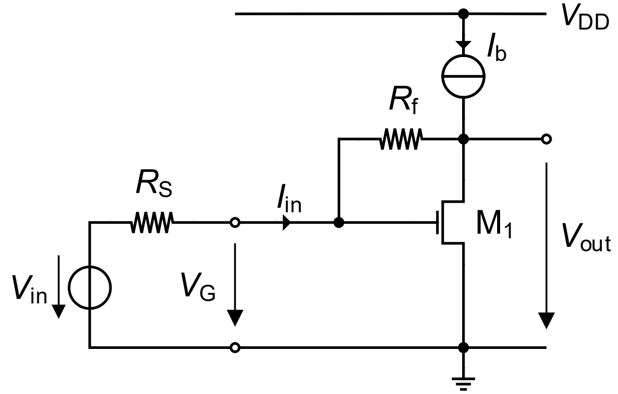
- And the noise factor F

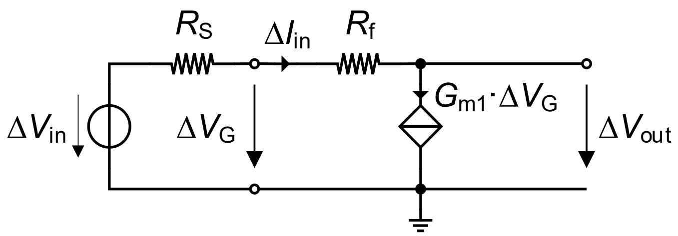
$$F(\omega_0) = \frac{R_{neq}(\omega_0)}{R_S} = 1 + \frac{\gamma_{nD} R_S C_{GS}^2 \omega_0^2}{G_m} = 1 + \frac{\gamma_{nD} R_S C_{GS} \omega_0^2}{\omega_t} = 1 + \frac{\gamma_{nD} \omega_0}{Q_L \omega_t} \quad \text{with} \quad Q_L = \frac{1}{\omega_0 R_S C_{GS}}$$

LNA Comparison

	Remark	LNA1	LNA2	LNA3	LNA4	LNA5
						
R_{in}	-	R_P	$\frac{R_P}{1+Q^2}$	$\frac{1}{G_{ms}}$	$\frac{1}{G_{ms}(1+Q^2)}$	$\frac{G_m L_S}{C_{GS}}$
G_{meq}	matched	$\frac{G_m}{2}$	$(1+jQ)\frac{G_m}{2}$	$-\frac{G_{ms}}{2}$	$(1+jQ)\frac{G_{ms}}{2}$	$\frac{\omega_t}{2R_S\omega_0}$
F	matched	$2+\frac{4\gamma_{nD}}{G_m R_S}$	$2+\frac{4\gamma_{nD}}{(1+Q^2)G_m R_S}$	$1+\delta_{nD}$	$1+\delta_{nD}$	$1+\frac{\gamma_{nD}\omega_0}{Q_L\omega_t}$
NF_{min}	minimum obtained without any current limitation, i.e. for G_m or $G_{ms}\rightarrow\infty$ and under matched conditions	3 dB	3 dB	1.8 dB	1.8 dB	0 dB !
NF_{50}	Value obtained for $Q<7$, $R_S=50\Omega$ and G_m or G_{ms} set by a bias current $I_b=100\mu A$	12.8 dB	3.7 dB (Q=7)	5.5 dB	1.8 dB	-

Resistive Feedback Wideband LNA





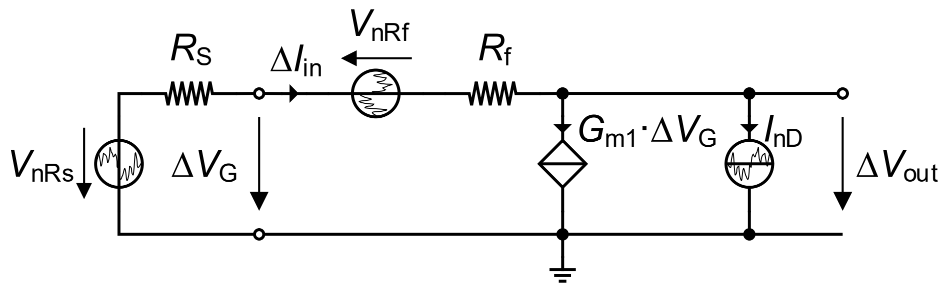
- The small-signal input impedance Z_{in} is given by $Z_{in} \triangleq \dfrac{\Delta V_G}{\Delta I_{in}} = \dfrac{1}{G_{m1}}$
- Impedance matching is therefore obtained by setting $G_{m1} = 1/R_S$
- The small-signal voltage gain is given by

$$A_v \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{G_{m1} \cdot R_f - 1}{G_{m1} \cdot R_S + 1} \qquad A_v\big|_{\text{matched}} = -\frac{R_f/R_S - 1}{2}$$

- In practice $R_f \gg R_S$ for which the gain reduces to

$$A_v \cong -\frac{G_{m1} \cdot R_f}{G_{m1} \cdot R_S + 1} \qquad A_v\big|_{\text{matched}} \cong -\frac{R_f}{2R_S}$$

Resistive Feedback Wideband LNA



- It can be shown that the input-referred thermal noise resistance is R_{neq} given by

$$R_{neq} = R_S + \left(\frac{G_{m1} \cdot R_S + 1}{G_{m1} \cdot R_f - 1}\right)^2 \cdot R_f + \left(\frac{R_f + R_S}{G_{m1} \cdot R_f - 1}\right)^2 \cdot G_{nD1} \cong R_S + \left(\frac{2R_S}{R_f}\right)^2 \cdot R_f + R_S^2 \cdot G_{nD1}$$

- where $G_{nD1} = \gamma_{nD1} \cdot G_{m1}$. The noise factor is then given by

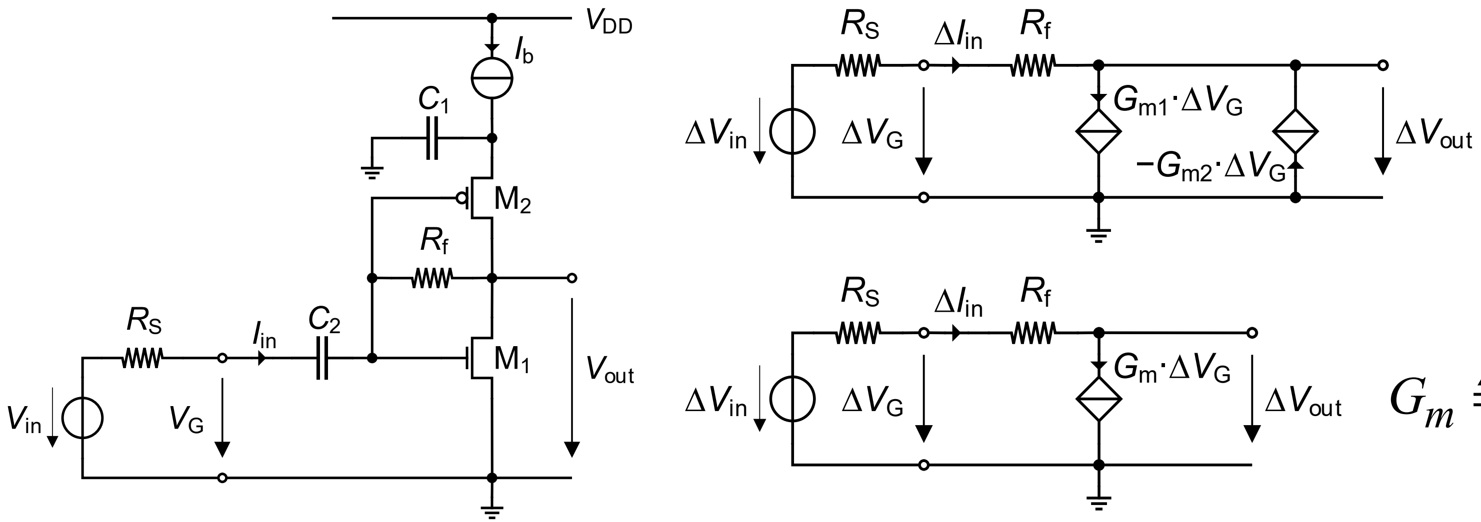
$$F = 1 + \left(\frac{G_{m1} \cdot R_S + 1}{G_{m1} \cdot R_f - 1}\right)^2 \cdot \frac{R_f}{R_S} + \left(\frac{R_f + R_S}{G_{m1} \cdot R_f - 1}\right)^2 \cdot \frac{G_{nD1}}{R_S} \cong 1 + \frac{4R_S}{R_f} + \gamma_{nD1}$$

- Assuming again that $R_f \gg R_S$ the noise factor further simplifies to

$$F \cong 1 + \gamma_{nD1}$$

- which again illustrates the importance of the transistor noise excess factor γ_{nD1}

Current Reuse LNA



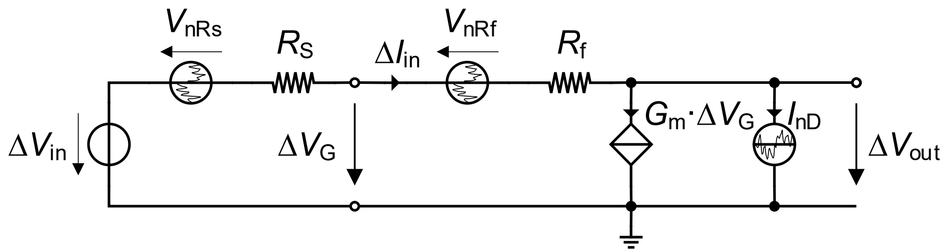
$$G_m \triangleq G_{m1} + G_{m2}$$

- As shown in the above small-signal schematics, the pMOS and nMOS transconductance come in parallel adding into a total transconductance $G_m = G_{m1} + G_{m2}$. Since M1 and M2 share the same bias current, G_m is about twice that obtained by a single transistor for the same bias current (particularly if both M1 and M2 are biased in WI)

- Merging the two transconductances results in the same schematic as the resistive feedback LNA. The input impedance Z_{in} and voltage gain are therefore given by

$$Z_{in} \triangleq \frac{\Delta V_G}{\Delta I_{in}} = \frac{1}{G_m} = \frac{1}{G_{m1} + G_{m2}} \qquad A_v \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{G_m \cdot R_f - 1}{G_m \cdot R_S + 1}$$

Current Reuse LNA



$$G_m \triangleq G_{m1} + G_{m2}$$

- The above noise schematic is identical to the resistive feedback LNA except for the transconductance and the noise current source I_{nD} which accounts for both the noise from M1 and M2
- Assuming again that $R_f \gg R_S$, the input-referred noise resistance is given by

$$R_{neq} \cong R_S + \left(\frac{2R_S}{R_f}\right)^2 \cdot R_f + R_S^2 \cdot G_{nD} = R_S + \frac{4R_S^2}{R_f} + R_S^2 \cdot \gamma \cdot G_m$$

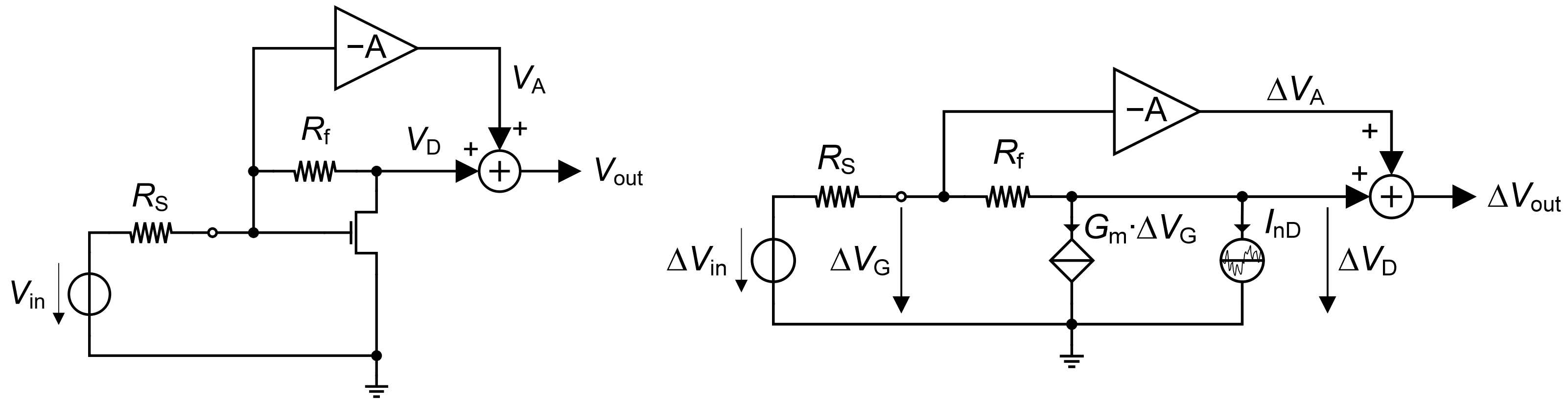
- where $G_{nD} \triangleq G_{nD1}+G_{nD2}$, $\gamma \triangleq (\gamma_{nD1} \cdot G_{m1} + \gamma_{nD2} \cdot G_{m2})/(G_{m1} + G_{m2})$ which is approximately $\gamma = \gamma_{nD1} = \gamma_{nD2}$ if $\gamma_{nD1} = \gamma_{nD2}$
- The noise factor under impedance matched condition $G_m = 1/R_S$ is then given by

$$F \cong 1 + \frac{4R_S}{R_f} + \gamma \cong 1 + \gamma \quad \text{for} \quad R_f \gg R_S$$

- The noise factor is identical to the resistive feedback LNA, but requires about half the current to achieve the same input impedance

Wide-band (WB) LNA with Noise Cancellation

- The noise of an LNA can be reduced by using feed-forward noise cancellation



- Gain is constructive for the input signal V_{in}

$$A_D = \frac{\Delta V_D}{\Delta V_{in}} = \frac{1 - G_m R_f}{1 + G_m R_S} \cong -\frac{R_f}{R_S}$$

$$A_A = \frac{\Delta V_A}{\Delta V_{in}} = \frac{-A}{1 + G_m R_S}$$

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = A_D + A_A = \frac{1 - A - G_m R_f}{1 + G_m R_S} \cong -\frac{A + G_m R_f}{1 + G_m R_S}$$

whereas it is destructive for the transistor noise source I_{nD}

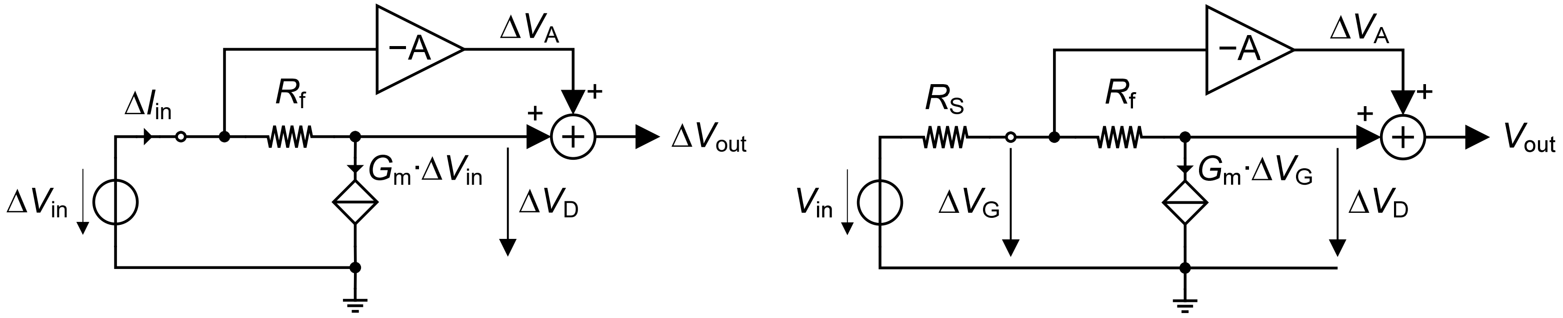
$$Z_{mD} = \frac{\Delta V_D}{I_{nD}} = -\frac{R_f + R_S}{1 + G_m R_S}$$

$$Z_{mA} = \frac{\Delta V_A}{I_{nD}} = \frac{A R_S}{1 + G_m R_S}$$

$$Z_m = \frac{\Delta V_{out}}{I_{nD}} = Z_{mD} + Z_{mA} = \frac{A R_S - \left(R_f + R_S\right)}{1 + G_m R_S}$$

F. Bruccoleri, E. A. M. Klumperink and B. Nauta, JSSC, Feb. 2004.

WB LNA with Noise Cancellation – Optimum Gain



- There is an optimum value of A for which the transistor noise is cancelled at the output (or equivalently $Z_m = 0$)

$$A_{opt} = 1 + \frac{R_f}{R_S} \quad \text{which leads to:} \quad A_{vopt} = -\frac{R_f}{R_S}$$

- The input impedance is easily calculated as

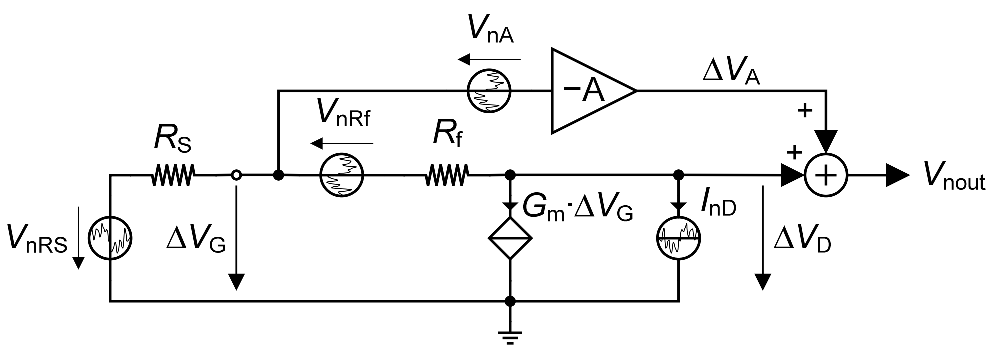
$$Z_{in} = \frac{\Delta V_{in}}{\Delta I_{in}} = \frac{1}{G_m}$$

- For input matching condition ($Z_{in} = R_S$), the optimum voltage gain A_{vopt} is then given by

$$A_{vopt} = -\frac{R_f}{R_S} = -G_m R_f$$

📖 F. Bruccoleri, E. A. M. Klumperink and B. Nauta, JSSC, Feb. 2004.

WB LNA with Noise Cancellation – Noise Figure



$$S_{V_{nA}} = 4kTR_{nA} \quad \text{with} \quad R_{nA} = \frac{\gamma_A}{G_{mA}}$$

- The noise figure can be calculated accounting for the noise added by the amplifier and the resistances

$$F = 1 + F_{G_{nD}} + F_{R_f} + F_{R_{nA}}$$

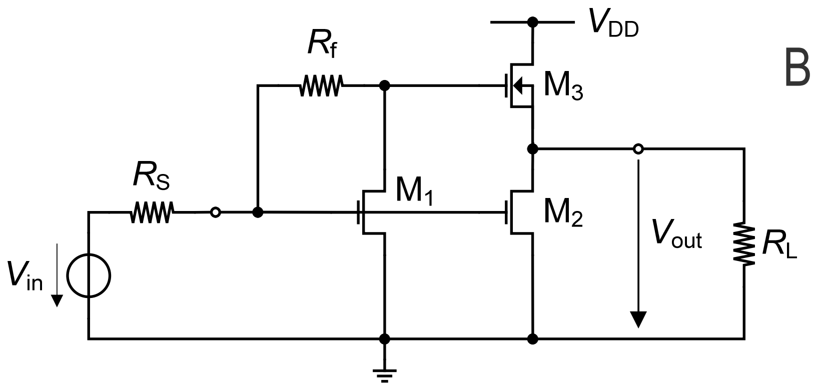
$$F_{G_{nD}} = \left(\frac{1 + R_f/R_S - A}{A - 1 + G_m R_f}\right)^2 \cdot G_{nD} R_S \quad F_{R_{nA}} = \left(\frac{A(1 + G_m R_S)}{A - 1 + G_m R_f}\right)^2 \frac{R_{nA}}{R_S} \quad F_{R_f} = \left(\frac{1 + G_m R_S}{A - 1 + G_m R_f}\right)^2 \frac{R_f}{R_S}$$

- Imposing $A = A_{opt} = 1 + R_f/R_S$ results in $F_{GnD} = 0$ and hence

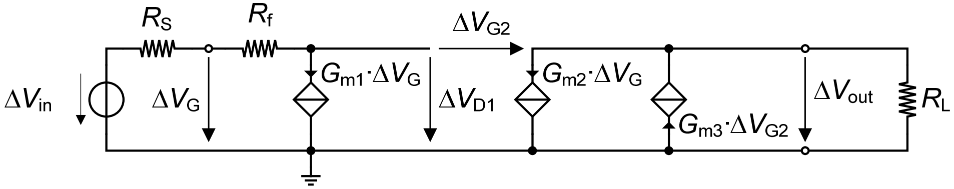
$$F_{opt} = 1 + \frac{R_S}{R_f} + \left(1 + \frac{R_S}{R_f}\right)^2 \cdot \frac{R_{nA}}{R_S} = 1 + \frac{R_S}{R_f} + \left(1 + \frac{R_S}{R_f}\right)^2 \cdot \frac{\gamma_A}{G_{mA} R_S}$$

F. Bruccoleri, E. A. M. Klumperink and B. Nauta, JSSC, Feb. 2004.

WB LNA with Noise Cancellation – Implementation



Bias circuit not shown



- Same result as before with $A = G_{m2}/G_{m3}$ and assuming $G_{m3}R_L \gg 1$

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{G_{m2}/G_{m3} + G_{m1}R_f - 1}{(1+G_{m3}R_L)(1+G_{m1}R_S)} G_{m3}R_L \cong -\frac{G_{m2}/G_{m3} + G_{m1}R_f - 1}{1+G_{m1}R_S} \cong -\frac{G_{m2}/G_{m3} + G_{m1}R_f}{1+G_{m1}R_S}$$

- The noise contributed by M1 is cancelled for

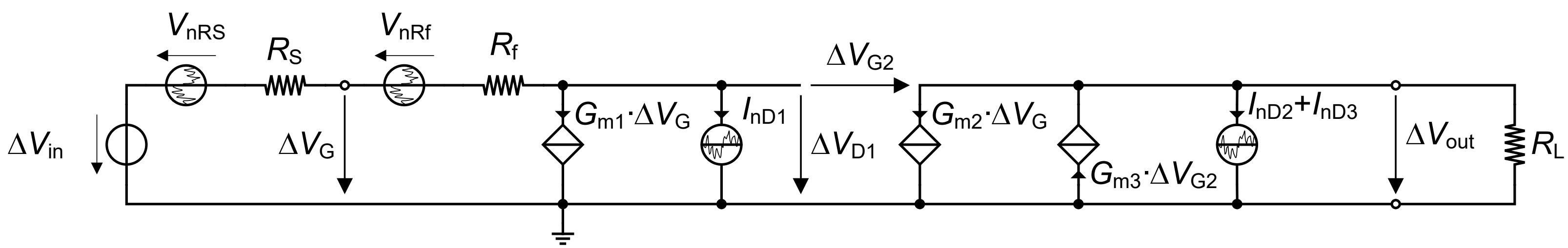
$$A = \frac{G_{m2}}{G_{m3}} = A_{opt} = 1 + \frac{R_f}{R_S} \cong \frac{R_f}{R_S} \quad \text{for:} \quad R_f \gg R_S$$

- The voltage gain then becomes

$$A_{vopt} = -\frac{G_{m3}R_L}{1+G_{m3}R_L}\frac{R_f}{R_S} \cong -\frac{R_f}{R_S} \quad \text{for:} \quad G_{m3}R_L \gg 1$$

F. Bruccoleri, E. A. M. Klumperink and B. Nauta, JSSC, Feb. 2004.

WB LNA with Noise Cancellation – Implementation



- The optimum noise factor obtained for $G_{m2}/G_{m3} = A_{opt} = 1 + R_f/R_S$ is then given by

$$F_{opt} = 1 + \frac{R_S}{R_f} + \frac{(G_{nD2} + G_{nD3}) R_S}{(G_{m3} R_f)^2} = 1 + \frac{R_S}{R_f} + \frac{\gamma_{nD2}(1 + R_S/R_f) + \gamma_{nD3} R_S/R_f}{G_{m3} R_f}$$

- Since $R_S/R_f \cong 1/|A_{vopt}| \ll 1$, the noise of M3 can be neglected compared to the one of M2, resulting in

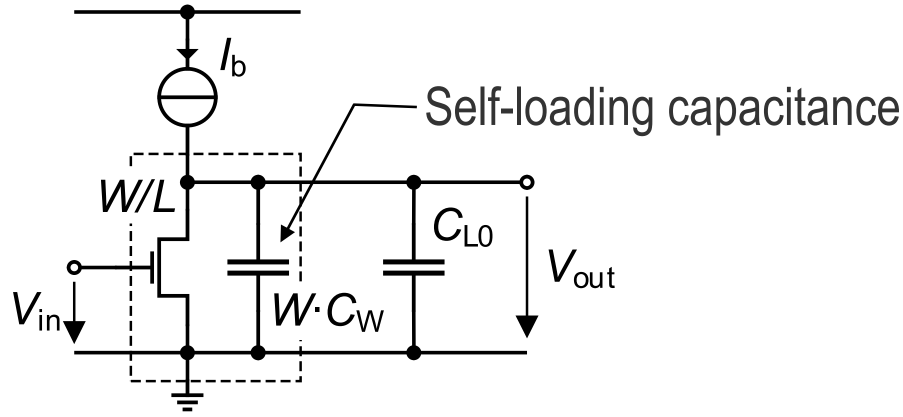
$$F_{opt} \cong 1 + \frac{R_S}{R_f} + \frac{\gamma_{nD2}}{G_{m3} R_f}$$

F. Bruccoleri, E. A. M. Klumperink and B. Nauta, JSSC, Feb. 2004.

Outline

- Low-Noise Amplifiers
- Low-power LNA Design

Current Optimization in a CS Stage (without VS)



- The voltage gain at high frequency ($\omega \gg \omega_u / A_{dc} = G_{ds}/C_L$) is given by

$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{G_m}{\omega C_L} = \frac{\omega_u}{\omega}$$

- where $\omega_u = G_m / C_L$ is the **gain-bandwidth** product
- We would like to find the **minimum current** for achieving a given voltage gain A_v at a given frequency ω
- This optimization of the bias current requires to include the self-loading capacitance that scales with W in the load capacitance $C_L = C_{L0} + W \cdot C_w$

📖 T. Melly, EPFL PhD Thesis No. 2231, 2000.
📖 A.-S. Porret, EPFL PhD Thesis No. 2542, 2002.
📖 A. Mangla, M. A. Chalkiadaki, F. Fadhuile, T. Taris, Y. Deval, and C. C. Enz, Microelectronics Journal, vol. 44, pp. 570-575, July 2013.

Current Optimization in a CS Stage (without VS)

- The bias current can be written in terms of the inversion coefficient IC and transistor aspect ratio W/L as

$$I_b = I_{spec\square} \cdot \frac{W}{L} \cdot IC$$

- The gain A_v or gain-bandwidth product ω_u is given by $\omega_u = G_m/C_L$ where the transconductance can also be written in terms of IC and W/L as

$$G_m = \frac{I_{spec\square}}{nU_T} \cdot \frac{W}{L} \cdot g_{ms}(IC) \quad \text{with} \quad g_{ms}(IC) = \frac{\sqrt{4IC+1}-1}{2} = \frac{2IC}{\sqrt{4IC+1}+1}$$

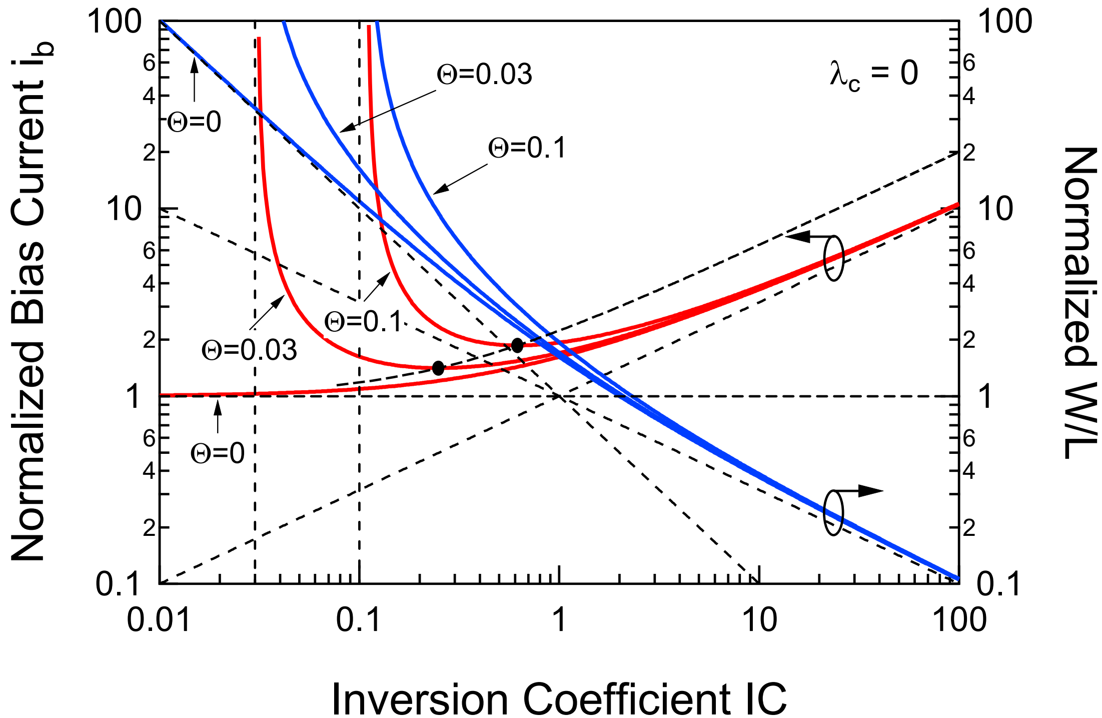
- The above equations can be solved for I_b and W/L, giving the following normalized equations

$$i_b \triangleq \frac{I_b}{I_{spec\square}} \frac{1}{\Omega} = \frac{IC}{g_{ms} - \Theta} \qquad \Omega \triangleq \frac{\omega_u}{\omega_L} \quad \omega_u \triangleq \frac{G_m}{C_L} \quad \omega_L \triangleq \frac{I_{spec\square}}{nU_T \cdot C_{L0}}$$

$$AR \triangleq \frac{W}{L} \cdot \frac{1}{\Omega} = \frac{1}{g_{ms} - \Theta} \qquad \Theta \triangleq \frac{\omega_u}{\omega_{tspec}} \quad \omega_{tspec} \triangleq \frac{I_{spec\square}}{nU_T \cdot C_W \cdot L}$$

📖 C. C. Enz and A. Pezzotta, MIXDES 2016.
📖 C. Enz, F. Chicco, and A. Pezzotta, IEEE Solid-State Circuits Magazine, vol. 9, no. 4, pp. 73-81, Autumn 2017.

Minimum Bias Current (without VS)



$$\Theta \triangleq \frac{\omega_u}{\omega_{tspec}}$$

$$\omega_u \triangleq \frac{G_m}{C_L}$$

$$\omega_{tspec} \triangleq \frac{I_{spec\square}}{nU_T \cdot C_W \cdot L}$$

- Self-loading cannot be ignored and introduces a **minimum bias current** for achieving a given gain-bandwidth product
- For reasonable values of the gain, the minimum current is achieved for an inversion coefficient in the moderate inversion region

📖 C. C. Enz and A. Pezzotta, MIXDES 2016.
📖 C. Enz, F. Chicco, and A. Pezzotta, IEEE Solid-State Circuits Magazine, vol. 9, no. 4, pp. 73-81, Autumn 2017.

Optimum IC for Minimum Bias Current (without VS)

- The **optimum** IC, assuming no VS, for which the bias current is minimum is given by

$$IC_{opt} = 2\Theta \cdot (1+\Theta) + (1+2\Theta) \cdot \sqrt{\Theta \cdot (1+\Theta)} \cong 2\Theta + \sqrt{\Theta} \quad \text{since} \quad \Theta \ll 1$$

- There is a minimum IC below which the specified gain-bandwidth ω_u can no more be achieved (assuming no VS)

$$IC_{lim} = \Theta \cdot (\Theta + 1) \cong \Theta$$

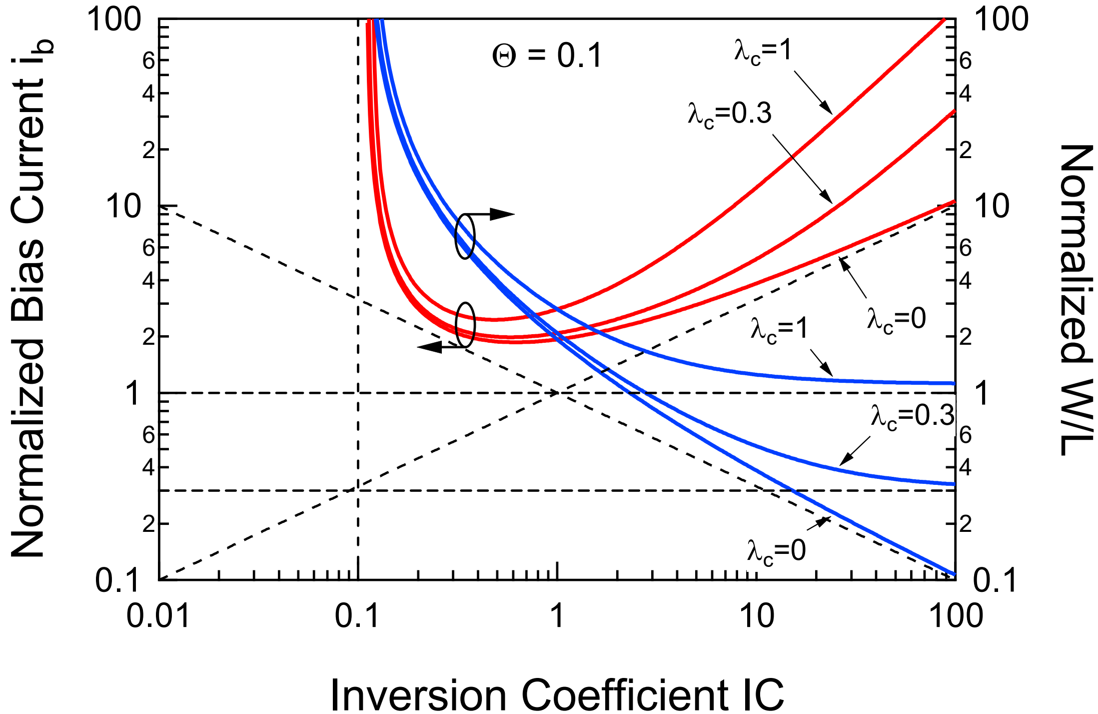
- This value corresponds to the vertical lines in the previous plot
- The normalized gain-bandwidth can be written as

$$\Omega = \frac{W/L}{1+\kappa \cdot W/L} \cdot g_{ms} \cong \frac{g_{ms}}{\kappa} \quad \text{for} \quad \frac{W}{L} \gg 1 \quad \text{where} \quad \kappa \triangleq \frac{C_w \cdot L}{C_{L0}}$$

- The above condition on IC also corresponds to the maximum gain-bandwidth that can be reached for a given IC (again assuming no VS)

$$\Omega_{max} = \frac{\sqrt{4IC+1}-1}{2\kappa}$$

Constant Gain-Bandwidth Product ω_u (with VS)

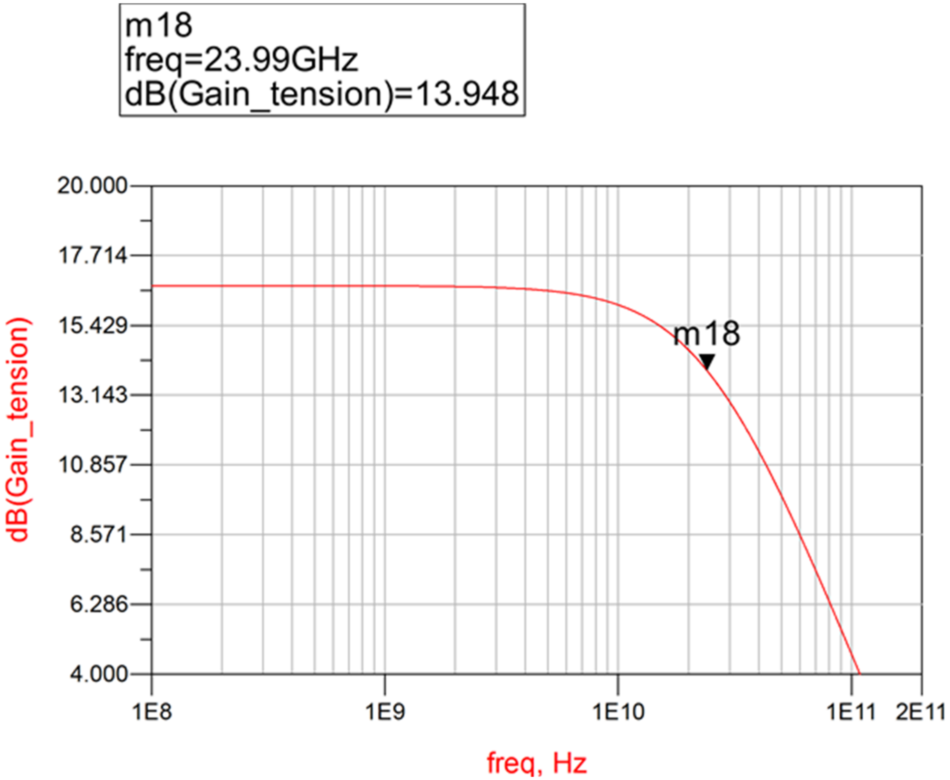


- The current saving is even greater when accounting for VS
- The optimum IC is slightly reduced due to VS and the minimum bias current is slightly increased

📖 C. C. Enz and A. Pezzotta, MIXDES 2016.
📖 C. Enz, F. Chicco, and A. Pezzotta, IEEE Solid-State Circuits Magazine, vol. 9, no. 4, pp. 73-81, Autumn 2017.

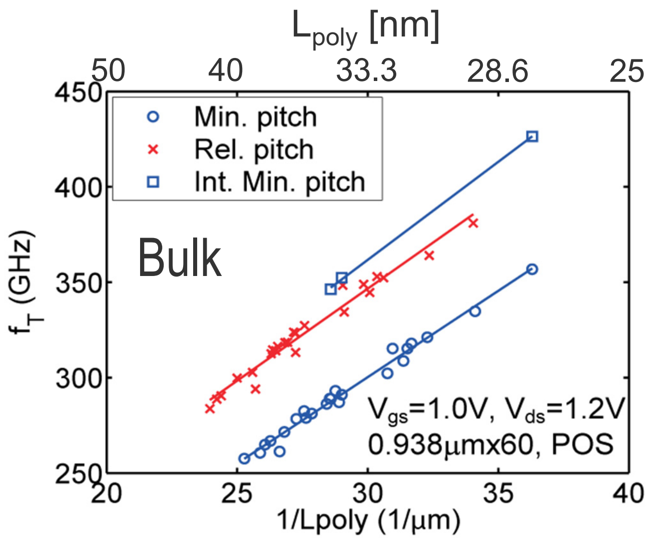
Example: 24GHz Amplifier in 40nm

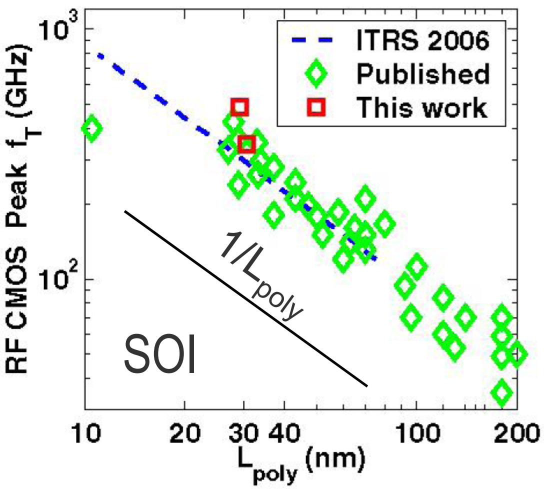
- Target: A_v=15dB at ω=24GHz with C_L=18.5 fF gives Ω=0.83
- For $L=L_{min}$=40nm (ℓ=1) we have IC_{opt}=6.3, i_{bopt}=8.78 and w_{opt}=1.41
- Denormalizing for the given 40nm technology parameters and plugging the values in the BSIM6 model leads to a simulated gain of 14dB at 24GHz
- Verification with ADS and BSIM6



A. Mangla, M. A. Chalkiadaki, F. Fadhuile, T. Taris, Y. Deval, and C. C. Enz, Microelectronics Journal, vol. 44, pp. 570-575, July 2013.

Low-power LNA Design





- High-f_t of deep-submicron CMOS process can be traded against power consumption by moving operating point to moderate or even weak inversion
- Similar to low-frequency analog design, the power consumption of RF LNA can be optimized using the normalized current efficiency factor

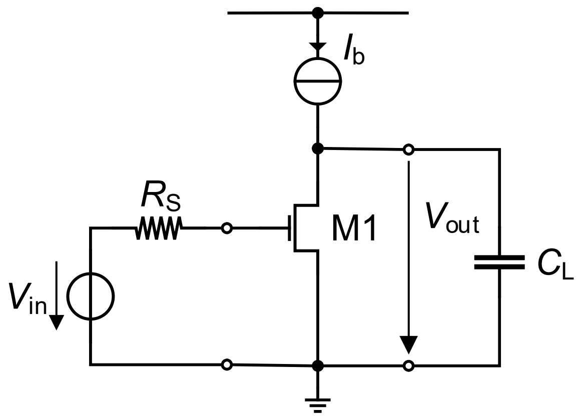
$$\text{current efficiency} \triangleq \frac{G_m \cdot n \cdot U_T}{I_D}$$

Hongmei Li, *et al.*, VLSI Symposium 2007

Sungjae Lee, *et al.*, IEDM 2007

Figure-of-Merit for Low Power RF

- The **voltage gain** and **noise factor** of a common-source stage loaded by a similar stage (i.e. having a fan-out FO equal to 1 and hence $C_L = C_{GS}$) are given by



$$A_v \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} \cong -\frac{G_m}{G_{ds} + j\omega C_L} \cong -\frac{G_m}{j\omega C_L} = j\frac{\omega_u}{\omega}$$

where $\omega_u \cong \frac{G_m}{C_L} = \frac{G_m}{C_{GS}} \cong \omega_t$ assuming $FO = 1$

$$F = 1 + \frac{\gamma_{nD}}{G_m R_S}$$

(assuming thermal noise from transistor M1 and resistance R_S only)

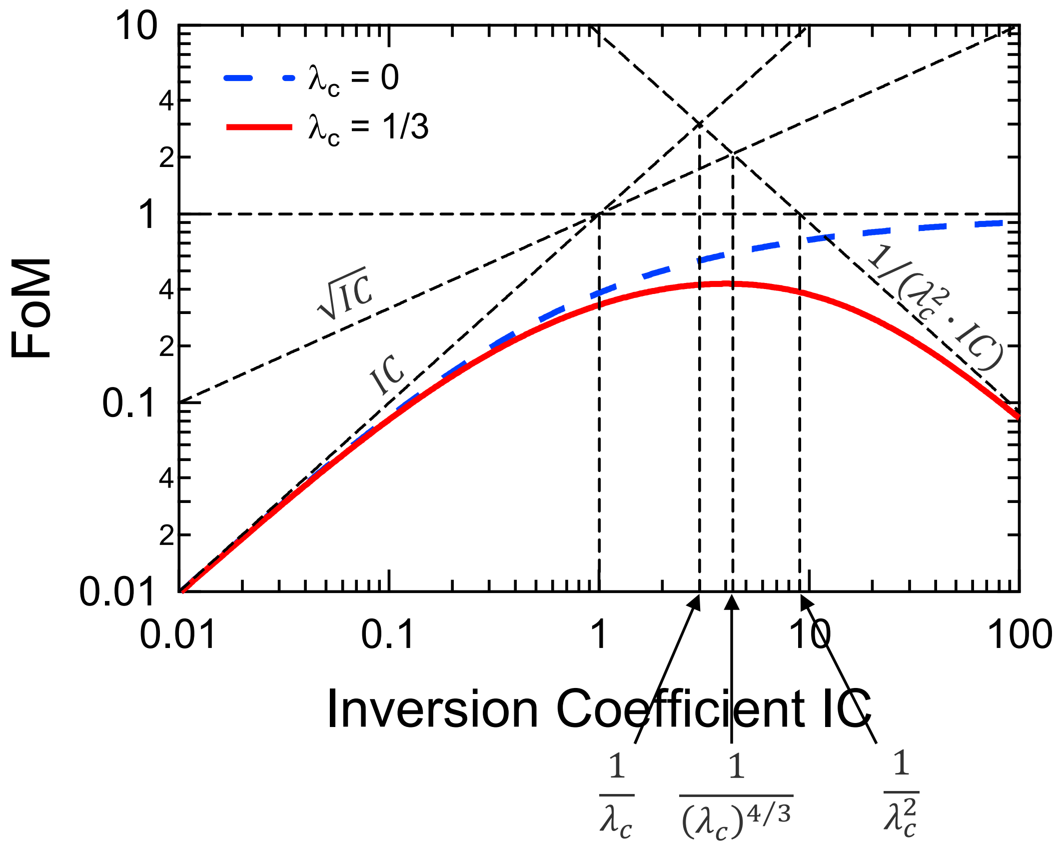
- A FoM can be defined in order to **maximize the gain-bandwidth product** and **minimize the noise factor** at a **given current**

$$FoM \triangleq \frac{\omega_u}{(F-1)\cdot I_b} \cong \frac{R_S}{\gamma_{nD}} \cdot \boxed{\frac{G_m \cdot \omega_t}{I_b}}$$

- This FoM is proportional to the $G_m / I_b \cdot \omega_t$ ratio, which is an important FoM for low-power RF IC design

📖 A. Shameli and P. Heydari, *ISLPED* 2006
📖 T. Taris, *et al.*, RFIC 2011
📖 A. Mangla, J.-M. Sallese and C. Enz, MIXDES 2011

The $G_m/I_D \cdot F_t$ FoM is Maximum in Moderate Inversion



$$\lambda_c = \frac{1}{3}$$

$$\frac{1}{\lambda_c} = 3$$

$$\frac{1}{\lambda_c^2} = 9$$

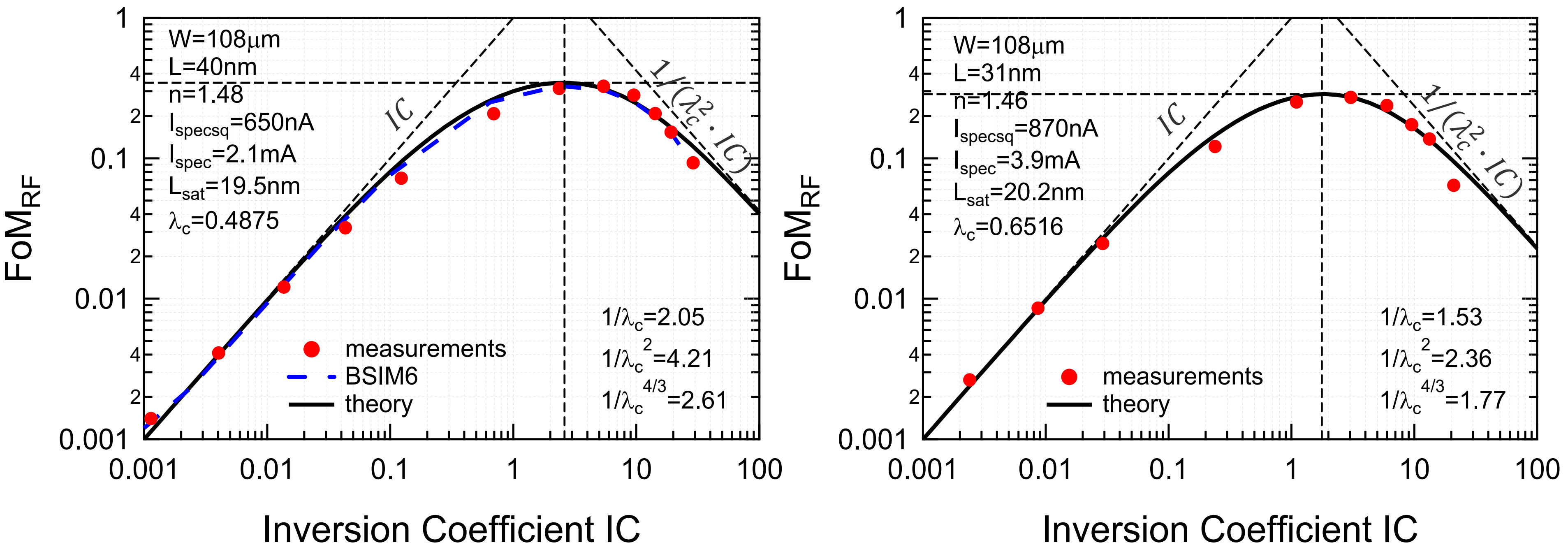
$$IC_{opt} \approx \frac{1}{\lambda_c^{4/3}} = 4.33$$

$$FoM_{opt} \approx FoM(IC_{opt}) = 0.43$$

$$FoM_{RF} = \frac{g_{ms} \cdot \Omega_t}{IC} = \frac{g_{ms}^2}{IC} = \frac{1}{IC} \cdot \left(\frac{\sqrt{(\lambda_c \cdot IC + 1)^2 + 4IC} - 1}{\lambda_c \cdot (\lambda_c \cdot IC + 1) + 2} \right)^2 \cong \begin{cases} IC & \text{WI} \quad IC \ll 1 \\ 1 & \text{SI without VS} \quad IC \gg 1 \text{ and } \lambda_c = 0 \\ \frac{1}{\lambda_c^2 \cdot IC} & \text{SI with VS} \quad IC \gg 1 \end{cases}$$

C. Enz and M. A. Chalkiadaki, APMC 2015.

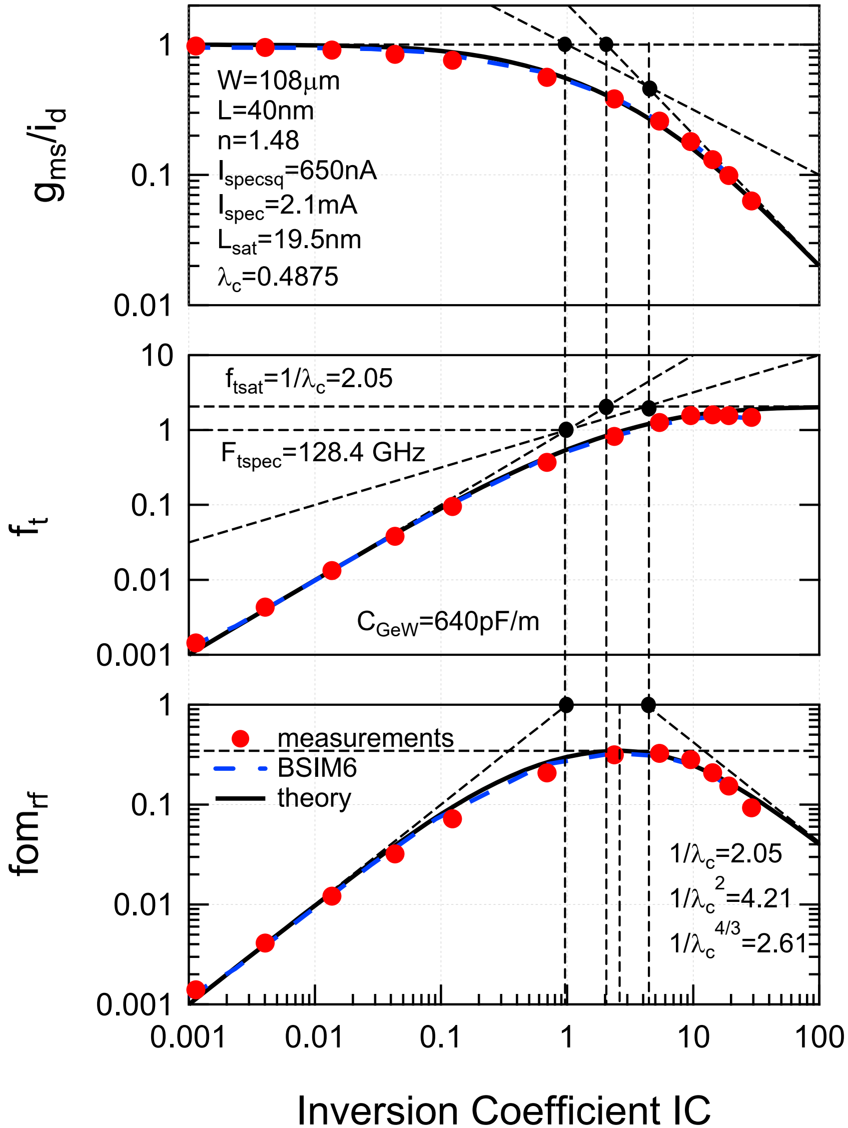
The $G_m/I_D \cdot F_t$ FoM vs. IC for 40nm and 28nm Bulk CMOS

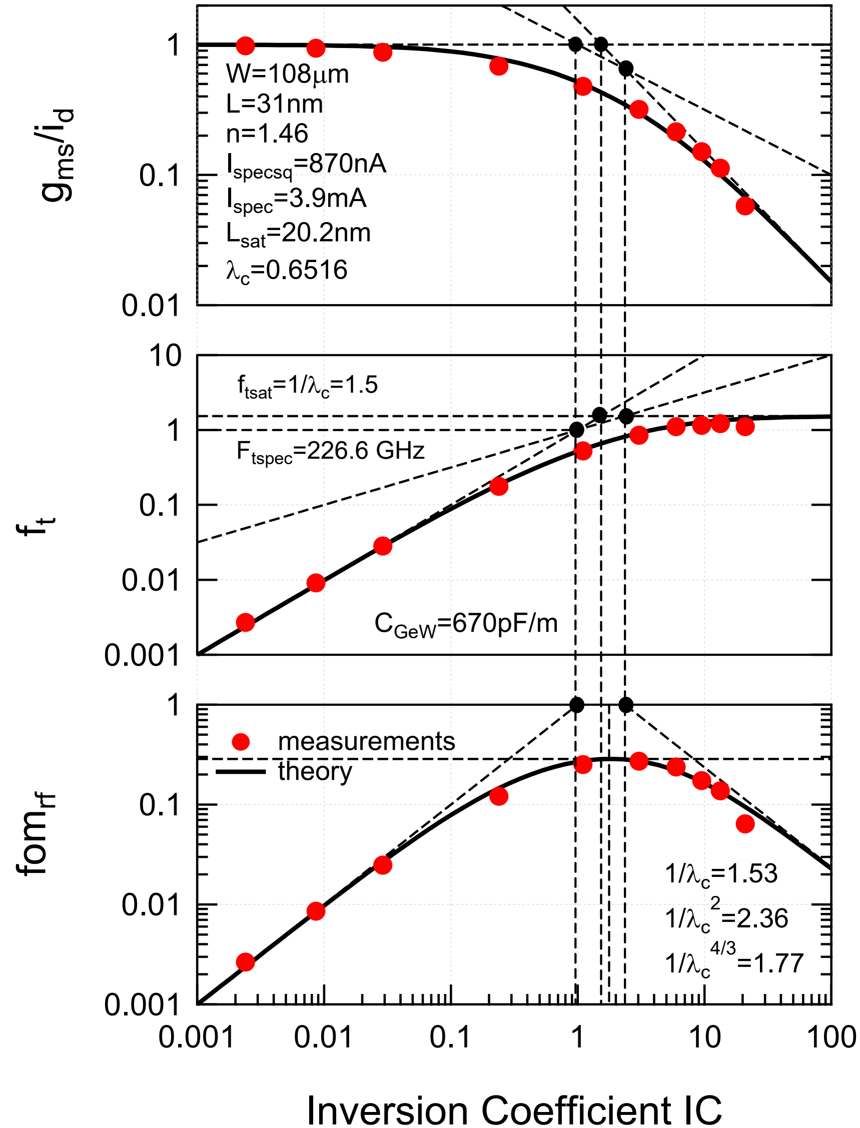


$$FoM_{RF} = \frac{g_{ms} \cdot \Omega_t}{IC} = \frac{g_{ms}^2}{IC} = \frac{1}{IC} \cdot \left(\frac{\sqrt{(\lambda_c \cdot IC + 1)^2 + 4IC} - 1}{\lambda_c \cdot (\lambda_c \cdot IC + 1) + 2} \right)^2$$

C. Enz and M. A. Chalkiadaki, APMC 2015.

Combined FoMs vs. IC for 40nm and 28nm Bulk CMOS



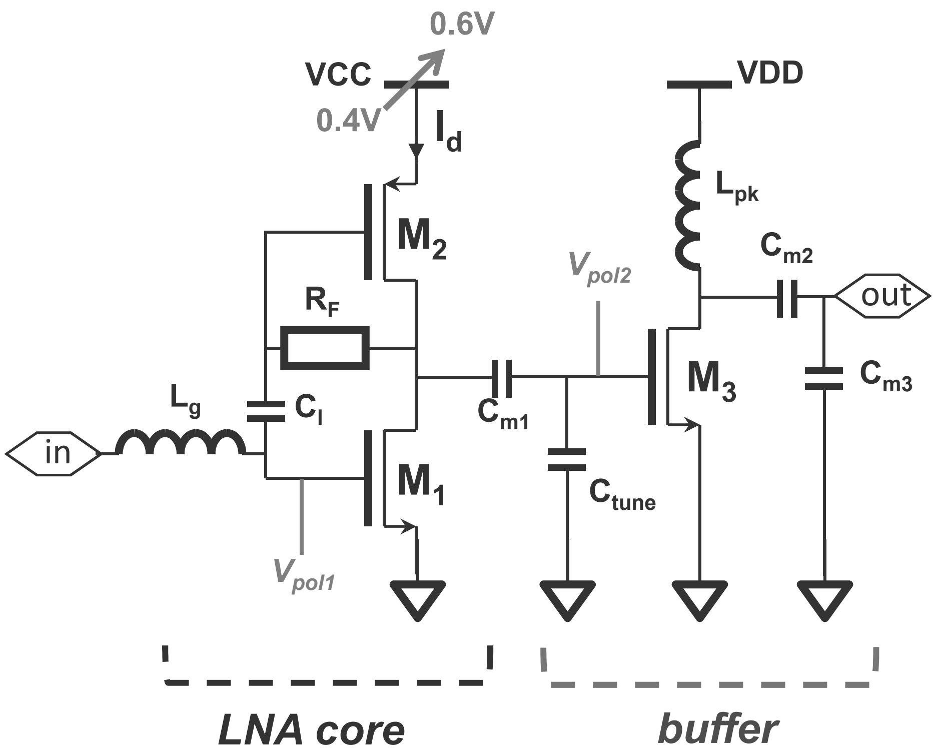


C. Enz and M. A. Chalkiadaki, APMC 2015.

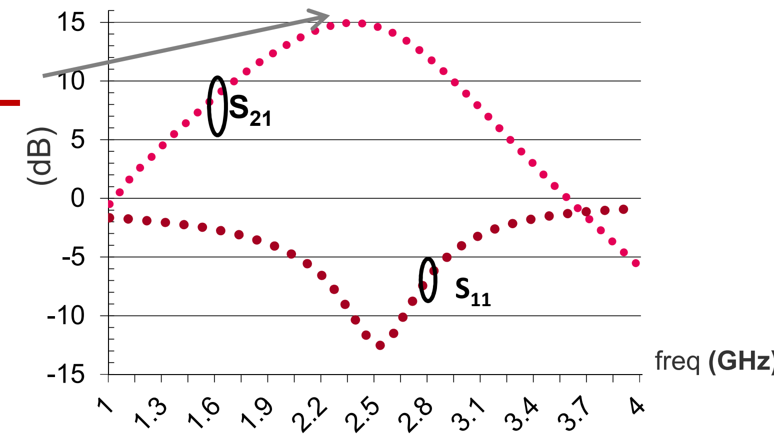
Ultra Low Power LNA – Maximize $G_m/I_D \cdot F_t$ FoM in MI

2.4 GHz LNA - CMOS 0.13µm

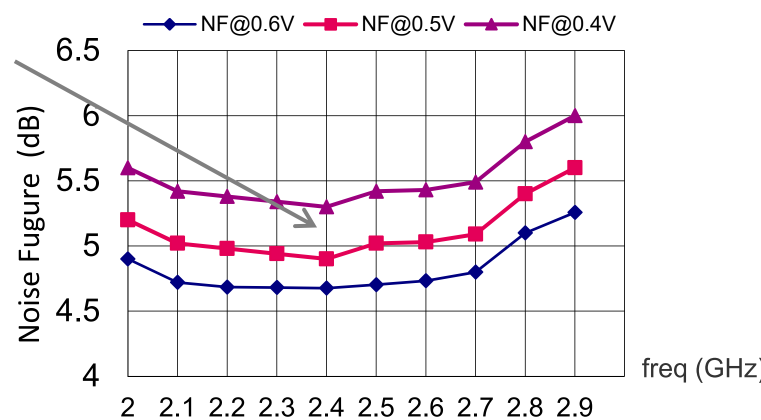
100µW@0.5V



15dB gain



4.8dB NF



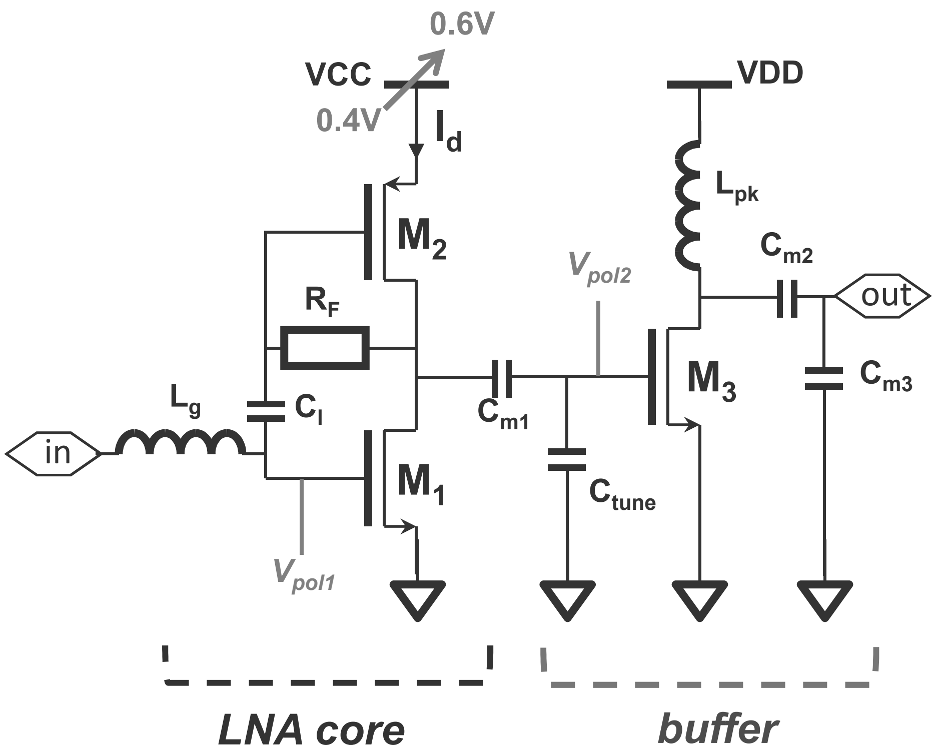
Transistors are biased in MI region to maximise FoM

📖 T. Taris, *et al.*, RFIC 2011

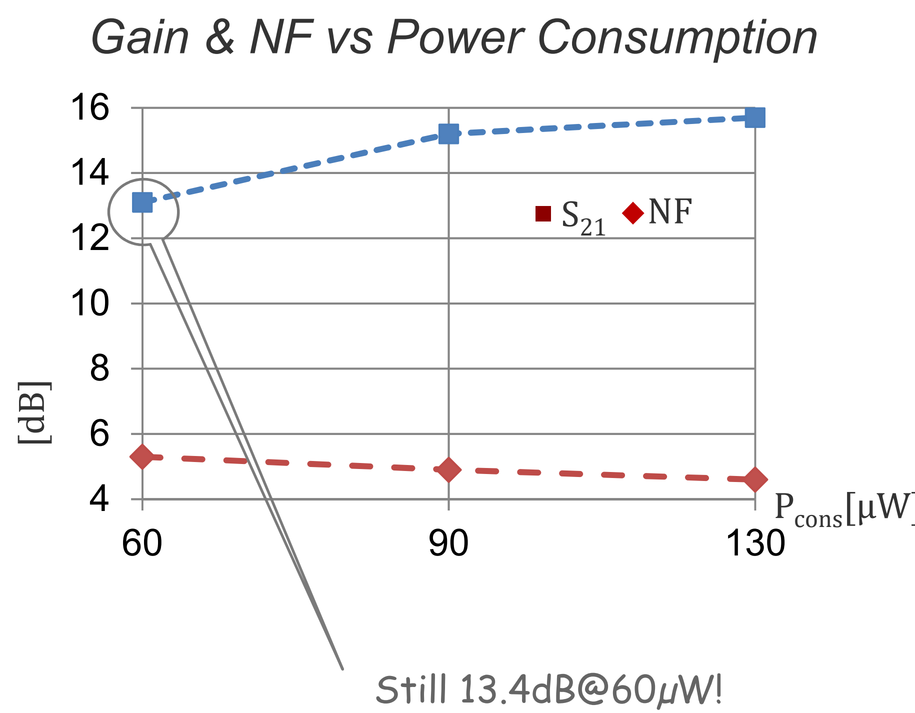
📖 Courtesy T. Taris, Univ. of Bordeaux, France

Ultra Low Power LNA – Maximize $G_m/I_D \cdot F_t$ FoM in MI

2.4 GHz LNA - CMOS 0.13µm



100µW@0.5V

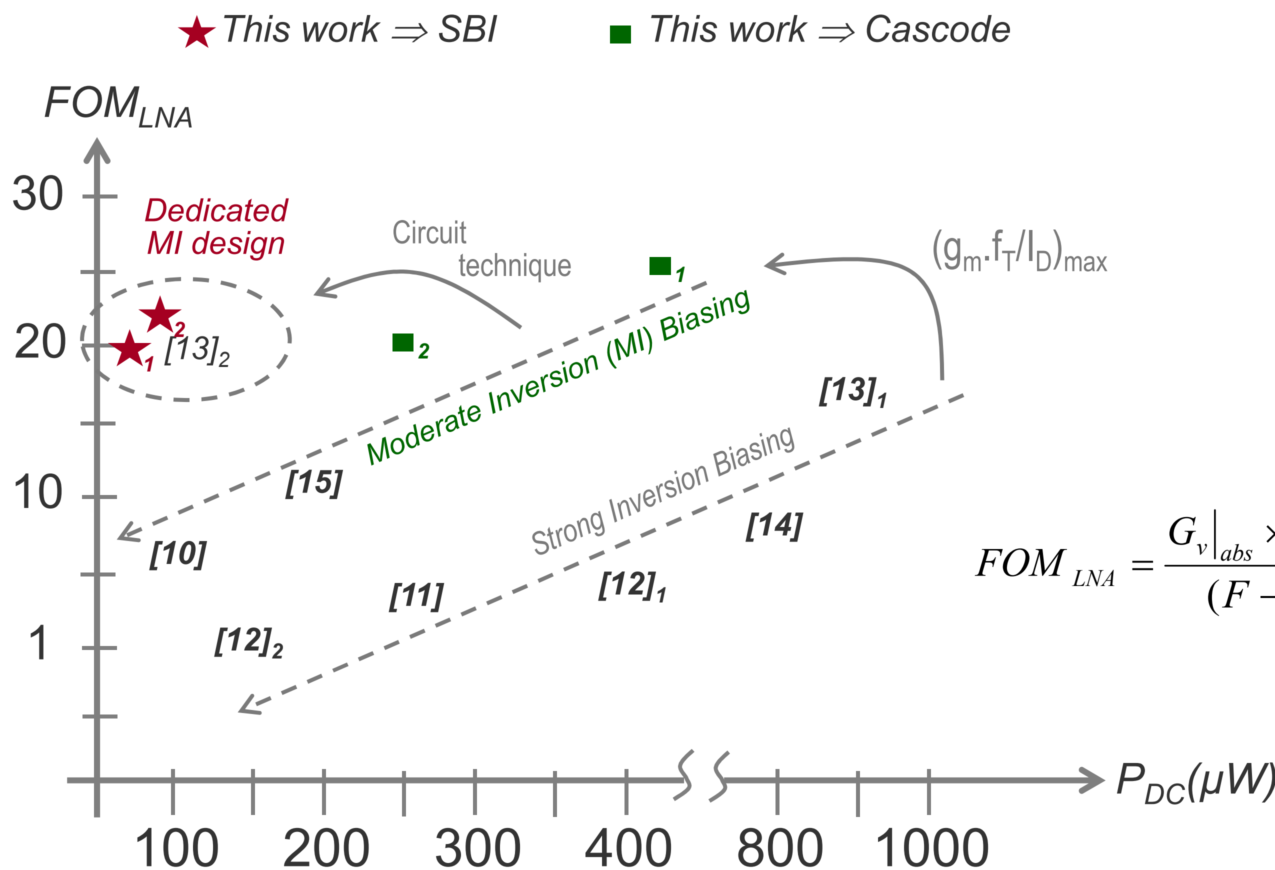


Transistors are biased in MI region to maximise FoM

T. Taris, *et al.*, RFIC 2011

Courtesy T. Taris, Univ. of Bordeaux, France

Ultra Low Power LNA – Comparison with SOTA



$$FOM_{LNA} = \frac{G_v\big|_{abs} \times IIP_3\big|_{mW} \times f_{RF}\big|_{GHz}}{(F-1)\big|_{abs} \times P_{cons}\big|_{mW}}$$

[10] A. Shameli"A novel Ultra Low Power Low Noise Amplifier using Differential Inductor Feedback", *IEEE ESSCIRC*, Montreux, Switzerland, Sep. 2006, pp.352-355

[11] B. G. Perumana, "A fully monolithic 260-µW, 1-GHz subthreshold low noise amplifier," *IEEE MiWCL*, Vol. 15, N°. 6, pp. 428-430, June 2005.

[12] H. Lee , "A 3 GHz subthreshold CMOS low noise amplifier," *IEEE RFIC Symposium*, San Francisco, CA, USA, June 2006, pp.545-548

[13] V. Aaron, « A subthreshold low-noise amplifier optimized for ultra-low -power applications in the ISM band", *IEEE MTT,* Vol. 56, N°2, pp. 286-292, feb. 2008

[14] J. Li, S. Hassan "A 0.7 V 850µW CMOS LNA for UHF RFID reader", *MOTL*, Vol. 52, N°12, pp. 2780-2782, dec. 2010

[15] C.J. Jeong, W. Qu, Y. Sun, D.Y. Soon, S.K. Han, S.G. Lee "A 1.5 V, 140 µA CMOS Ultra Low Power Common Gate LNA", *IEEE RFIC,* Baltimore, USA, June 2011, pp. 203-206

📖 T. Taris, *et al.*, RFIC 2011

📖 Courtesy T. Taris, Univ. of Bordeaux, France