Low-power radio design for the IoT
Exercise 4 (17.03.2022)

Christian Enz

Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland

Problem 1 Inductance Equations

We wish to design a 5 nH inductor, operating at 5 GHz and with a quality factor, Q, greater or equal to 10. Assume the sheet resistance of the top metal layer is 22 m$\Omega/\square$, the width, W, is kept equal to 4 µm while the spacing, S, to 0.5 µm.

- Determine the number of windings, N, which are needed if the total length of the inductor wire, l_{tot}, is assumed equal to 2000 µm. Then determine if the above value of Q is feasible by using this set of values.
- Design a spiral inductor operating at 900 MHz with $Q \geq 6$. Is the 5 nH structure of the previous point suitable for this application? What other choices do we have?

Problem 2 Inductor Design

To implement an inductor we would like to use metals 7, 8, and 9 in parallel, as shown in Fig. 1. Since metals 7 and 8 are typically half as thick as metal 9, the total metal resistance is lowered by about a factor of 2 by adding them.

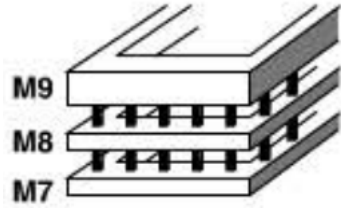

Figure 1: Inductor structure with parallel spirals on different metal layers.

- Design the same inductor of the second point of Problem 1 by assuming $W = 3$ µm, $S = 0.5$ µm, $N = 10$ and the stacked structure.
- Comment the effect on the parasitic capacitance with the substrate when the stacked structure is used.

Problem 3 MOS varactor capacitance

A MOS varactor realized in 65 nm technology has an effective length of 50 nm and an overlap capacitance, C_{ov}, of 0.09 fF/µm.

- Determine the largest capacitance range that the varactor can provide assuming the device width to be 1 µm and $C_{ox} = 17$ fF/µm^2.
- How would the maximum capacitance and its quality factor change if the device length is doubled?