Low-power radio design for the IoT
Exercise 4 (17.03.2022)

Christian Enz

Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland

Problem 1 Inductance Equations

We wish to design a 5 nH inductor, operating at 5 GHz and with a quality factor, Q, greater or equal to 10. Assume the sheet resistance of the top metal layer is 22 m$\Omega/\square$, the width, W, is kept equal to 4 µm while the spacing, S, to 0.5 µm.

- Determine the number of windings, N, which are needed if the total length of the inductor wire, l_{tot}, is assumed equal to 2000 µm. Then determine if the above value of Q is feasible by using this set of values.
- Design a spiral inductor operating at 900 MHz with $Q \geq 6$. Is the 5 nH structure of the previous point suitable for this application? What other choices do we have?

Problem 2 Inductor Design

To implement an inductor we would like to use metals 7, 8, and 9 in parallel, as shown in Fig. 1. Since metals 7 and 8 are typically half as thick as metal 9, the total metal resistance is lowered by about a factor of 2 by adding them.

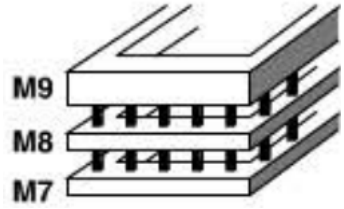

Figure 1: Inductor structure with parallel spirals on different metal layers.

- Design the same inductor of the second point of Problem 1 by assuming $W = 3$ µm, $S = 0.5$ µm, $N = 10$ and the stacked structure.
- Comment the effect on the parasitic capacitance with the substrate when the stacked structure is used.

Problem 3 MOS varactor capacitance

A MOS varactor realized in 65 nm technology has an effective length of 50 nm and an overlap capacitance, C_{ov}, of 0.09 fF/µm.

- Determine the largest capacitance range that the varactor can provide assuming the device width to be 1 µm and $C_{ox} = 17$ fF/µm^2.
- How would the maximum capacitance and its quality factor change if the device length is doubled?

Solutions to Exercise 4 (17.03.2022)

Problem 1 Inductance Equations

- Determine the number of windings, N, which are needed if the total length of the inductor wire, l_{tot}, is assumed equal to 2000 µm. Then determine if the above value of Q is feasible by using this set of values.

The quality factor of the inductor is given by Eq. (1).

$$Q = \frac{L\omega_0}{R_s} \tag{1}$$

where L is the inductance, ω_0 is the operating angular frequency, and R_s is the parasitic resistance. To solve this problem, first the inductor needs to be designed with the provided specifications in order to obtain the desired inductance. In particular, the inductors total length and the number of windings need to be set.

With numerous inductors used in a typical transceiver, it is desirable to have closed-form equations that provide the inductance value in terms of the spiral's geometric. The formula given in Eq.(2) has less tha 10% error for inductors in the range of 5 nH to 50 nH properties and with squared spirals:

$$L = 1.3 \times 10^{-7} \frac{A_m^{5/3}}{A_{tot}^{1/6} W^{1.75} (W+S)^{0.25}} \tag{2}$$

where A_m is the metal area and A_{tot} is the total inductor area. If the inductor total length l_{tot} is much greater than the spacing S, then l_{tot} can be approximated as in Eq. (3).

$$l_{tot} \approx 4N \left(\sqrt{A_{tot}} - W - (N-1)(W+S) \right) \tag{3}$$

By manipulating Eq. (2) with Eq. (3), Eq. (4) is obtained.

$$L = 1.3 \times 10^{-7} \frac{l_{tot}^{5/3}}{\left(\frac{l_{tot}}{4N} + W + (N-1)(W+S) \right)^{1/3} W^{0.083} (W+S)^{0.25}} \tag{4}$$

We observe that N appears only within the square brackets in the denominator, in two terms varying in opposite directions, with the result raised to the power of 1/3.

For example, if $l_{tot} = 2000\,\mu\text{m}$, then as N varies from 2 to 3 to 4 to 5, then inductance rises from 3.96 nH to 4.47 nH to 4.83 nH to 4.96 nH respectively. In order to get the desired 5 nH inductance L, $N = 5$ is selected. Then, the number of squares of this device is defined as in Eq. (5).

$$\square = \frac{l_{tot}}{W} = \frac{2000}{4} = 500 \tag{5}$$

After this, R_s can be calculated in order to derive Q. The wire consists of 500 squares and hence has a resistance R_s of $500 \times 22\,\text{m}\Omega/\square = 11\,\Omega$. By replacing ω_0, L and R_s in Eq. (1), $Q \approx 14.3$ is obtained, hence the value of needed value for Q is feasible with this set of values.

- Design a spiral inductor operating at 900 MHz with $Q \geq 6$. Is the 5 nH structure of the previous point suitable for this application? What other choices do we have?

Since $Q = L\omega_0/R_s$, if the frequency falls from 5 GHz to 900 MHz, the Q declines from 14.3 to 2.6 Thus, a value of 5 nH is inadequate for usage at 900 MHz. Let us attempt to raise the inductance, hoping that, in $Q = L\omega_0/R_s$ L can increase at higher rate than can R_s. Indeed, we observe from Eq. (4) that $L \propto l_{tot}^{5/3}$, whereas $R_s \propto l_{tot}$. For example, if $l_{tot} = 8\,\text{mm}$, $N = 10$, $W = 6\,\mu\text{m}$, and $S = 0.5\,\mu\text{m}$, then Eq. (4) yields $L \approx 35\,\text{nH}$. For a sheet resistance of $22\,\text{m}\Omega/\square$, $R_s = (8000\,\mu\text{m}/6\,\mu\text{m}) \times 22\,\text{m}\Omega/\square = 29.3\,\Omega$. Thus the Q reaches 6.75 at 900 MHz.

Problem 2 Inductor Design

- Design the same inductor of the second point of Problem 1 by assuming $W = 3\,\mu m$, $S = 0.5\,\mu m$, $N = 10$ and the stacked structure.

Since W is reduced from 6 µm to 3 µm, the term $(W + S)^{0.25}$ in the denominator of Eq. (4) falls by a factor of 1.17, requiring a similar drop in $l_{tot}^{5/3}$ in the numerator so as to obtain $L \approx 35\,nH$. Iteration yields $l\,l_{tot} \approx 6800\,\mu m$. The length and the outer dimension are smaller because the narrower metal line allows a tighter compaction of the turns. With three metal layers in parallel, we assume a sheet resistance of approximately $11\,m\Omega/\square$, obtaining $R_s = 25\,\Omega$ and hence a Q of 7.9. The parallel combination therefore yields a higher Q.

- Comment the effect on the parasitic capacitance with the substrate when the stacked structure is used.

The closer proximity of metal-7 to the substrate slightly raises the parasitic capacitance with the substrate.

Problem 3 MOS varactor capacitance

- Determine the largest capacitance range that the varactor can provide assuming the device width to be 1 µm and $C_{ox} = 17\,fF/\mu m^2$.

Assuming a width of 1 µm for the device, we have $2WC_{ov} = 17\,fF$ and the gate oxide capacitance of $17\,fF/\mu m^2 \times 1\,\mu m \times 50\,nm = 0.85\,fF$. Thus, the minimum capacitance is 0.18 fF (if the series combination of the oxide and depletion capacitances is neglected), and the maximum capacitance reaches $0.18\,fF + 0.85\,fF = 1.03\,fF$. The largest possible capacitance ratio is therefore equal to 5.72. In practice, the series combination of the oxide and depiction capacitances is comparable to $2WC_{ov}$, reducing this ratio to about 2.5.

- How would the maximum capacitance and its quality factor change if the device length is doubled?

In order to achieve a larger capacitance range, the length of MOS varactors can be increased. In the above example, if the effective channel length grows to 100 nm, then the capacitance ratio reaches $0.18\,fF + 1.7\,fF/0.18\,fF = 10.4$. However, the larger source-drain resistance results in a lower Q. Since the maximum capacitance goes from 1.03 fF to 1.88 fF and since the channel resistance is doubled, the Q $(= 1/(RC\omega))$ falls by a factor of 3.65. In other words, an m-fold increase in the channel length translates to roughly an m^2-fold drop in the Q.