Real Time Embedded Systems

Embedded System design example

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System to design, requests

- Softcore processor: NIOSII standard version
  - 4kiB instruction cache
  - no data cache
- Memories:
  - on-chip memory SRAM, 16 kiB with 32 bits width
  - epcs controller for external Flash memory
- Programmable interfaces:
  - JTAG UART for debug purpose
  - Parallel port **In 8 bits**
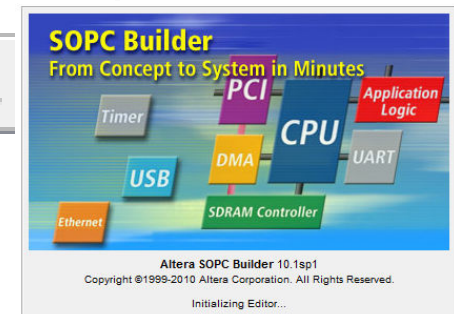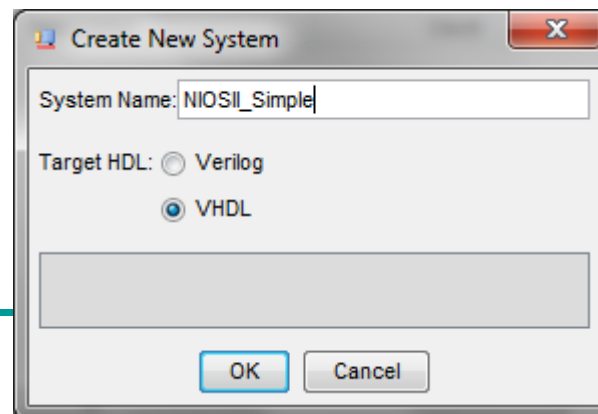 - Parallel port **Out 8 bits**

Design Environment

- Goal: Design of an Embedded system on FPGA
  - ➢ Specifically for Altera Cyclone device
  - ➢ System design with:
    - ➢SOPC or Qsys environment on QuartusII
  - ➢ VHDL for specific modules design
  - ➢ ModelSim-Altera simulation tools
  - ➢ Software in C with:
    - ➢ NIOS IDE (Legacy) or
    - ➢ NIOS SBT

General Bloc Schematic
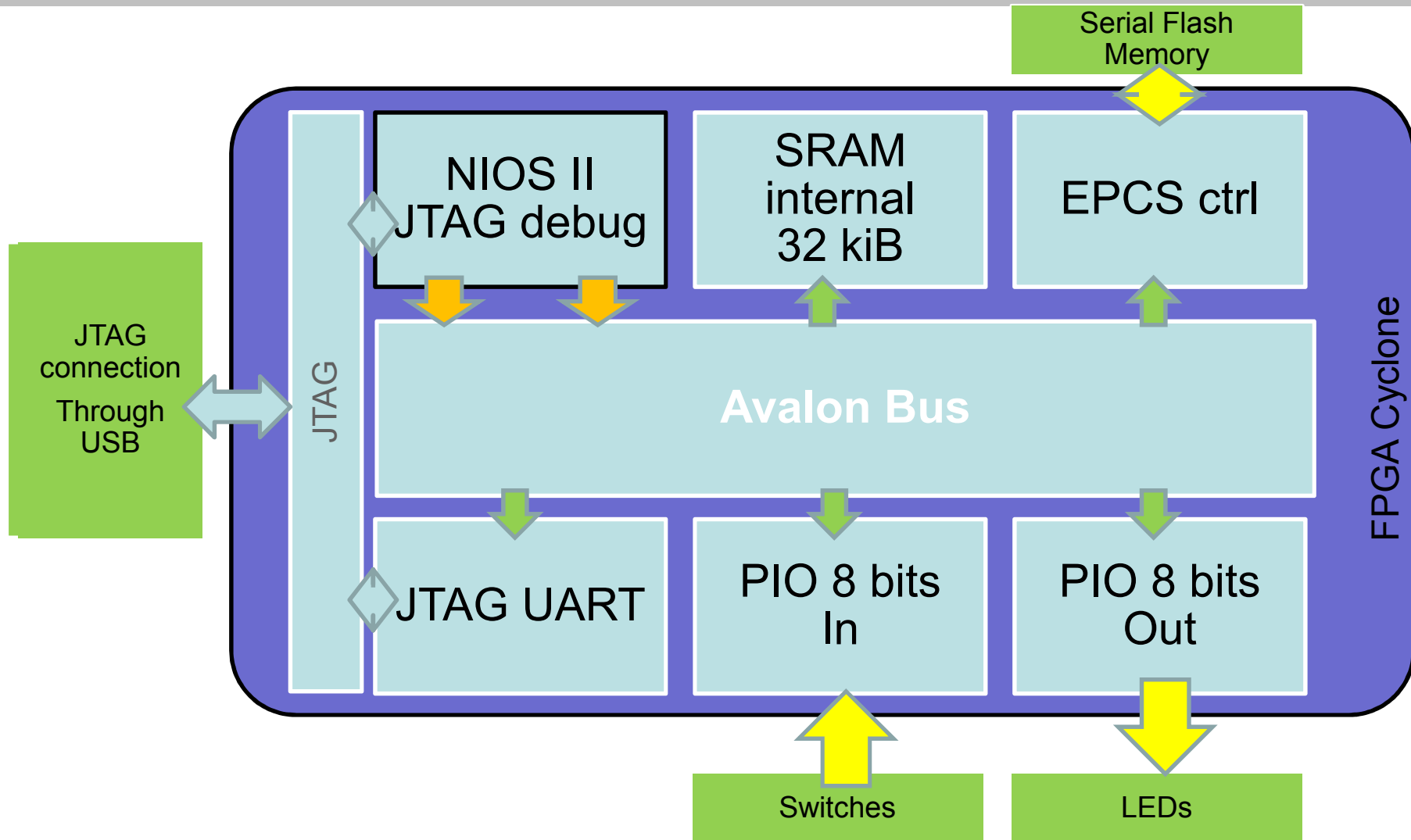
How to design it ?

- QuartusII ➔ New project
  - ➢ CycloneII -> EP2C20F484C8
- New schematic File
  - ➢ Files ➔ New ➔ Bloc Diagram/Schematic
  - ➢ Files ➔ Save as… (*Labo_NIOS_InOut.bdf*)
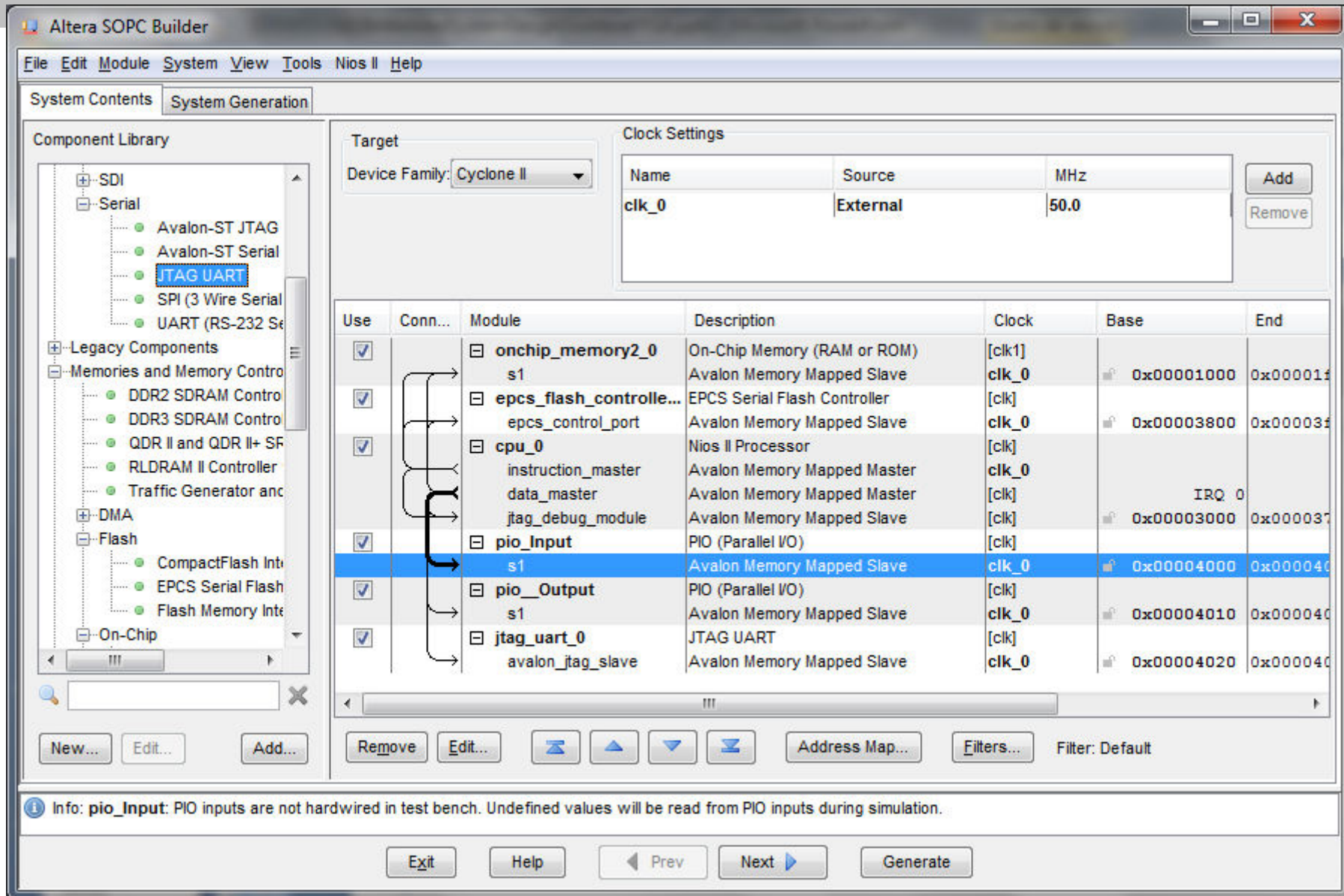- SOPC Builder/Qsys(clic-clic or
  - ➢ Select VHDL
  - ➢ Give a name

Create New System

System Name: NIOSII_Simple

Target HDL: ○ Verilog
○ VHDL

OK   Cancel

SOPC Add Components

- →Memories→ On-Chip → RAM 4kiBytes
- → Memories → Flash → EPCS Ctrl
- → Processors → NIOSII → /s
  - ➢Reset Vectors → On-Chip SRAM
  - ➢Interrupt Vectors → On-Chip SRAM
  - ➢Cache Instruction → 4kiB
  - ➢JTAG → Level 2

SOPC Add Components

- → Peripherals → uC Peripheral → PIO
  - ➤ 8 bits Input
  - ➤ 8 bits Output
- → Interface Protocols → Serial →
  - ➤ JTAG UART

- System → Auto Assign Base Addresses

SOPC View

System Generation

- ## Generate
  - ➤ Produce Avalon bus module and all the interconnections

- ## Include in the schematic
  - ➤ Add Pins Input/Output
  - ➤ Clk with PLL (24 MHz to 50MHz)
  - ➤ Tcl files for pin numbering

- ## Compile

- Correct the errors (if any)
- Nice ! The design is ready

- Download on the board
  - ➢(FPGA4U/robot or other)

- Run NIOSII IDE and write the software
  - ➢Copy In port on Out Port by software