Real Time Embedded Systems

" *Memories* "

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Chargé de cours

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Prof. HES

General classification of electronic memories

- **Non-volatile Memories**
  - ROM
  - PROM
  - EPROM
  - EEPROM
  - Flash EPROM
    - E lectrically
    - E rasable
    - P rogrammable
    - R ead
    - O nly
    - M emory

- **Volatile Memories**
  - Static RAM (RAM/SRAM)
    - S tatic
    - S ynchronous
  - Dynamic RAM (DRAM/SDRAM, DDR)
    - D ynamic
    - R andom
    - A ccess
    - M emory
    - S ynchronous
    - D ual
    - D ata R ate
  - Z-RAM (Zero transistor)

NVRAM
Non**V**olatile
RAM

MRAM
Magnetoresistive RAM

FRAM
Ferromagnetic RAM

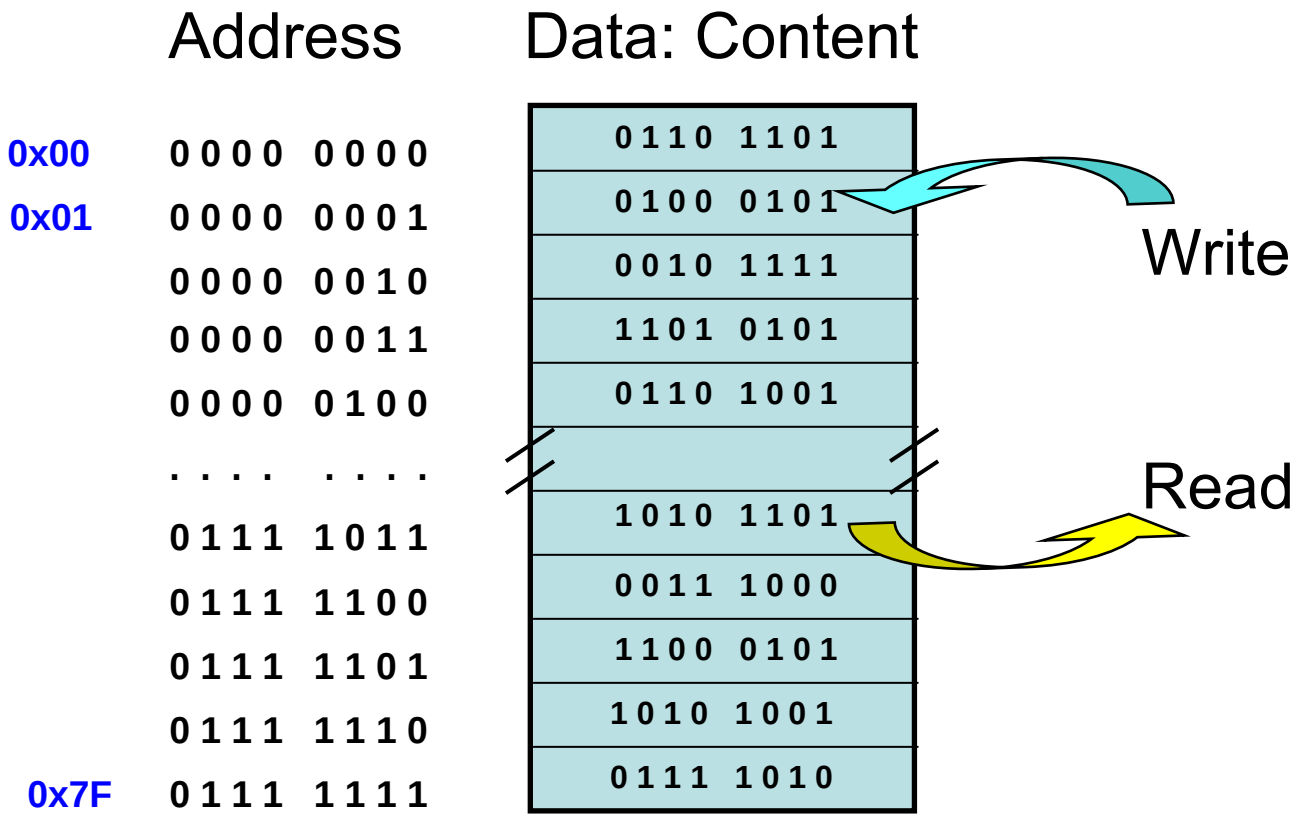
Objectives

- Having an overview of the different kinds of memories on the market
- Understanding the internal architecture of dynamic memories, specifically SDRAM

Memory Model

Random Access Memory :

at Address → DATA



Content

- Non Volatile Memories
- Volatiles Memories : Static
- Volatiles Memories : Dynamic
  - Asynchronous
  - Synchronous
  - Dual Data Rate
  - RamBus
  - Evolution / Market

Non Volatile Memories

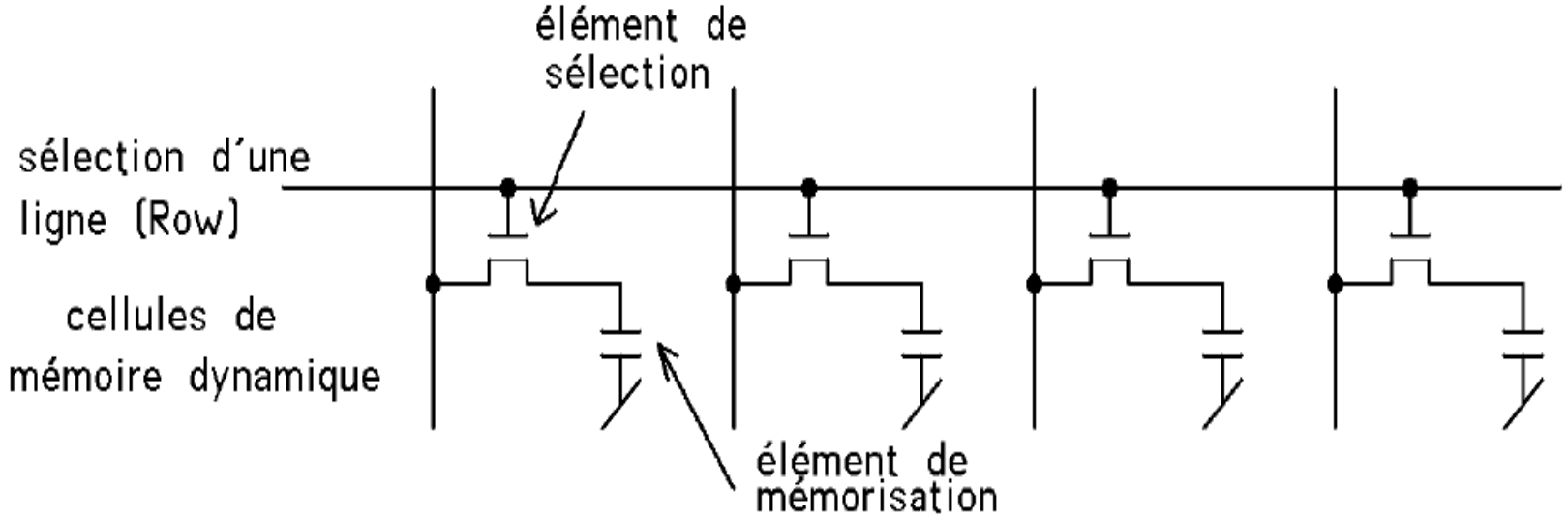
Volatile Memories

Dynamic Memories

DRAM (asynchronous basic memory)

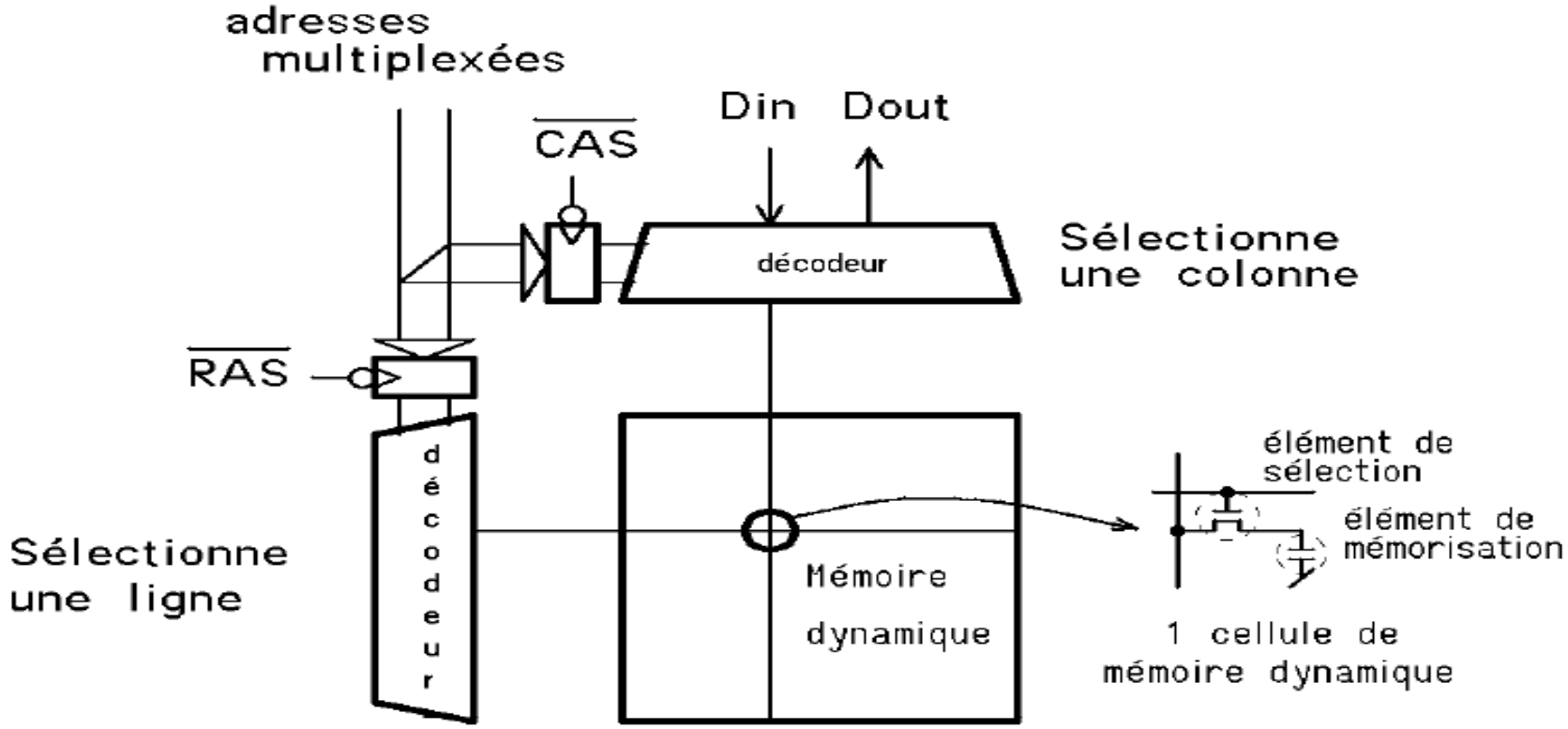
- Main characteristics:
  - Dynamic Memory
    - Rom/Column Organization
    - Control signals: /RAS, /CAS, /WR, (/OE)
  - Burst access possibilities:
    - Nibble mode
    - Static Column Mode
    - Page Mode
    - Fast Page Mode (FPM)
    - Extended Data Out (EDO)

DRAM



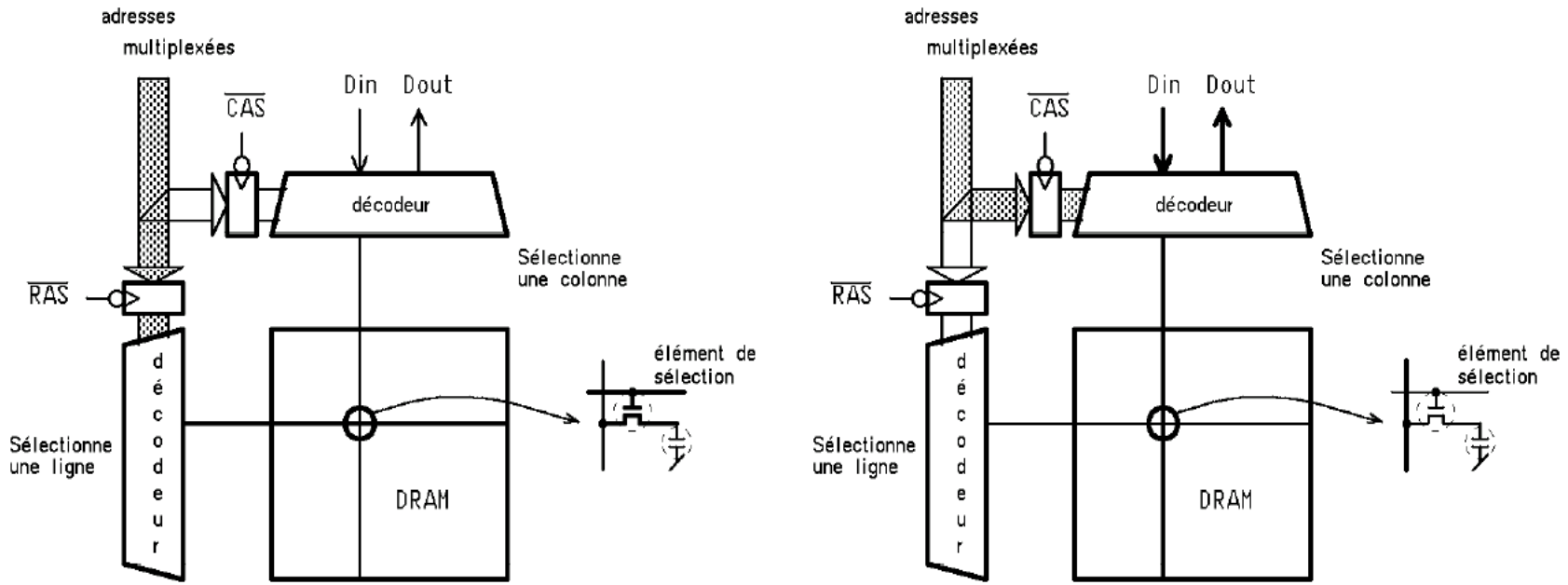
Memorization elements
All acceded on a row at the same time
→ Power consummation

DRAM



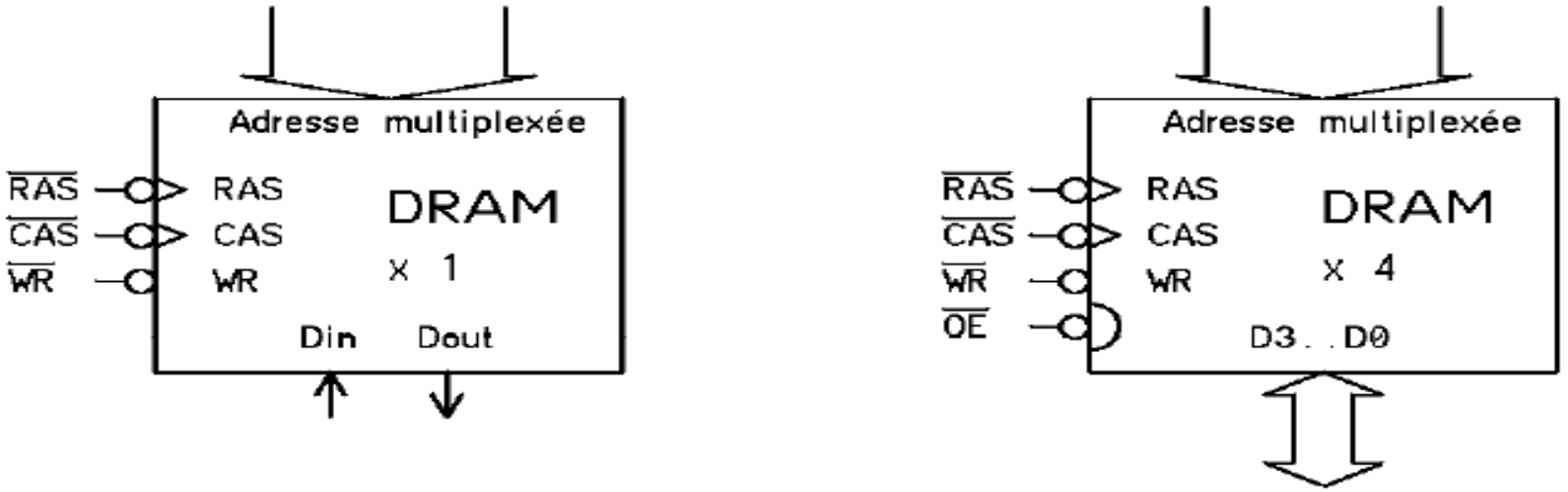
multiplexed Addresses: Row/Column

DRAM



multiplexed Addresses: Row/Column

DRAM

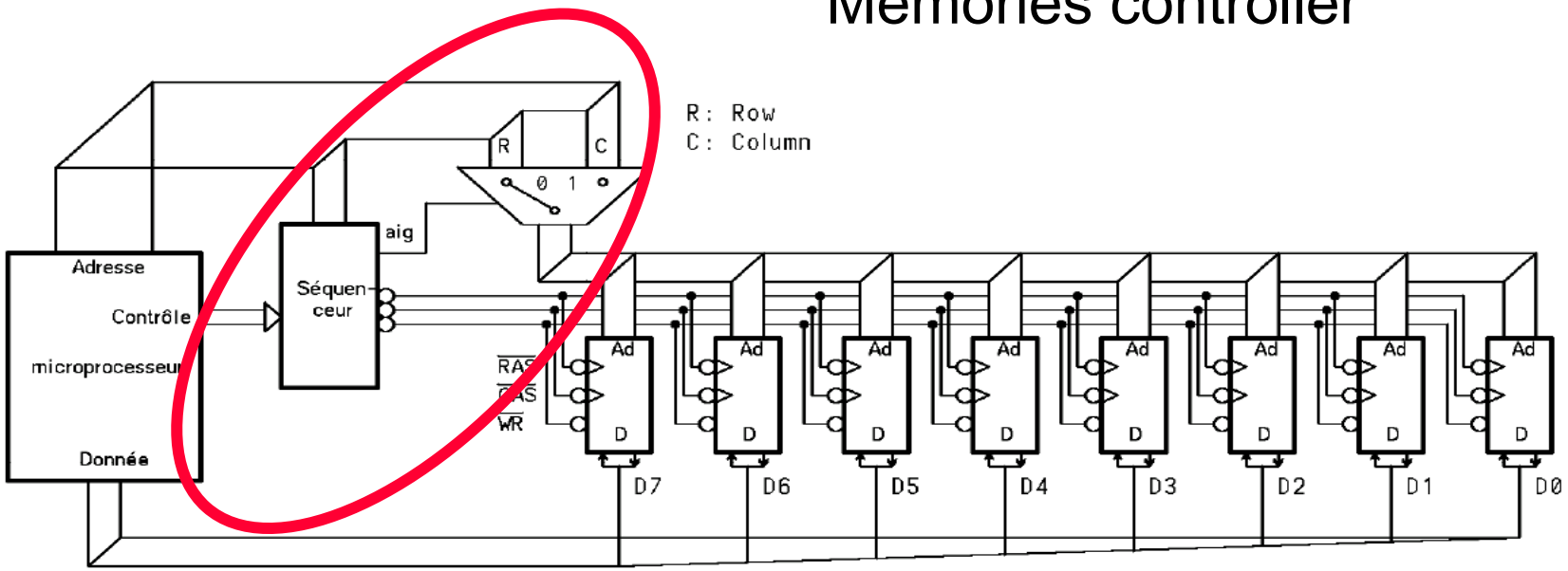


Data Bus :

- Separated In/Out
- Bi-directional

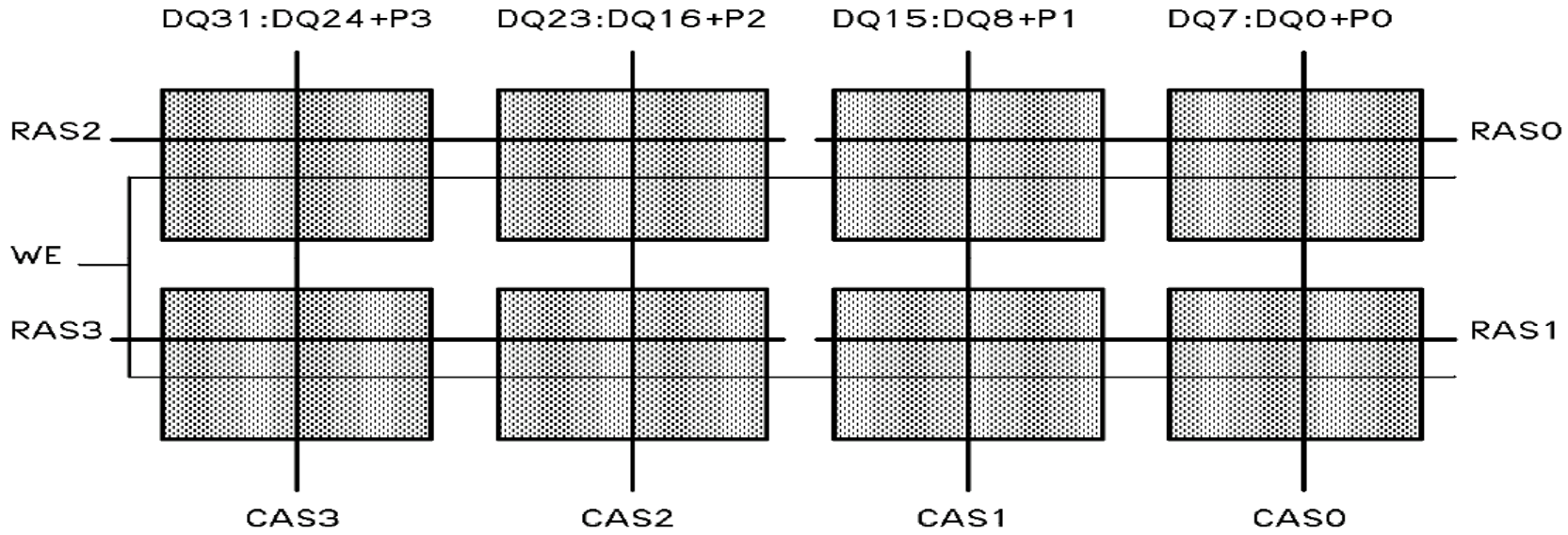
DRAM

Memories controller



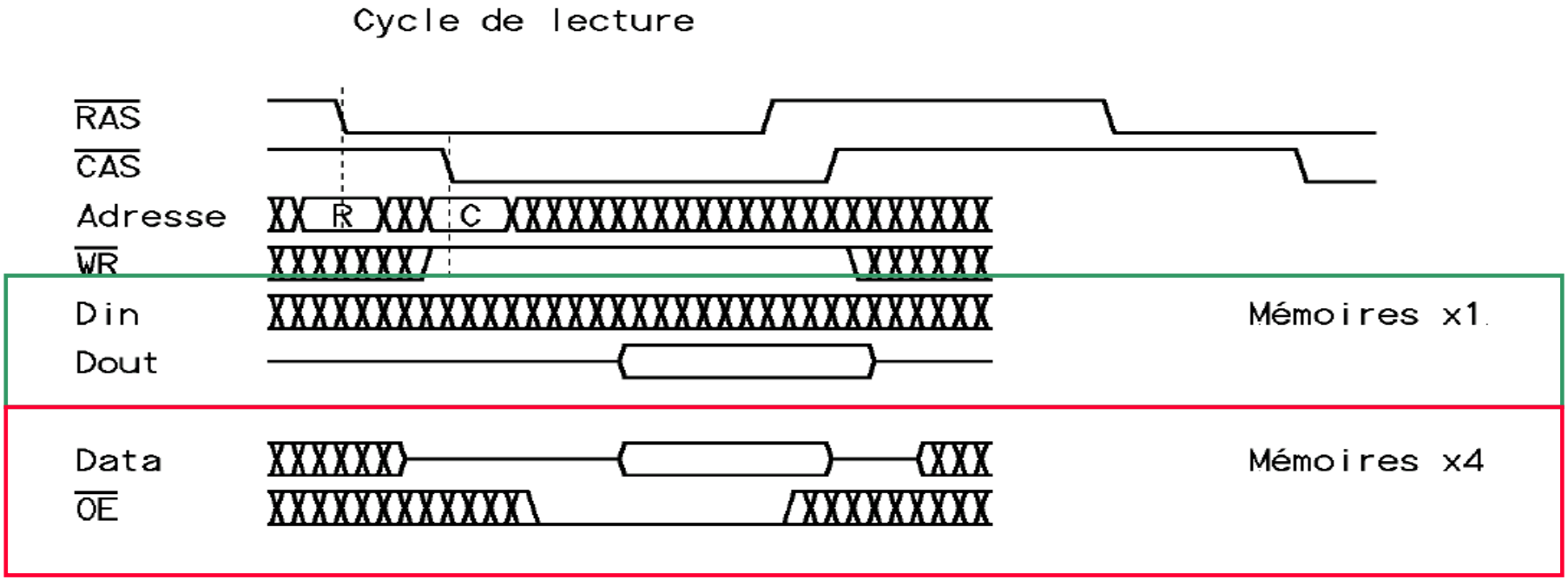
Processor interface : Address multiplexer

DRAM, circuits multiples

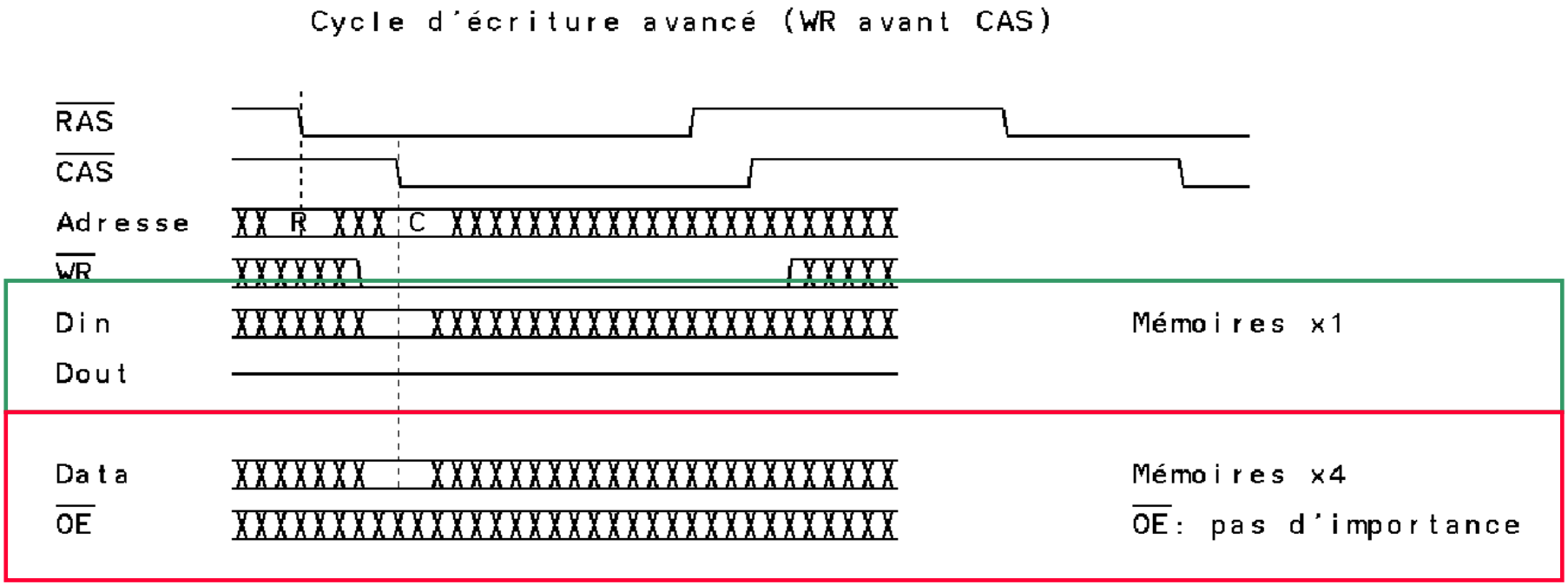


Control signals organization on a memory module
Ex: 32 bits data bus width, with parity

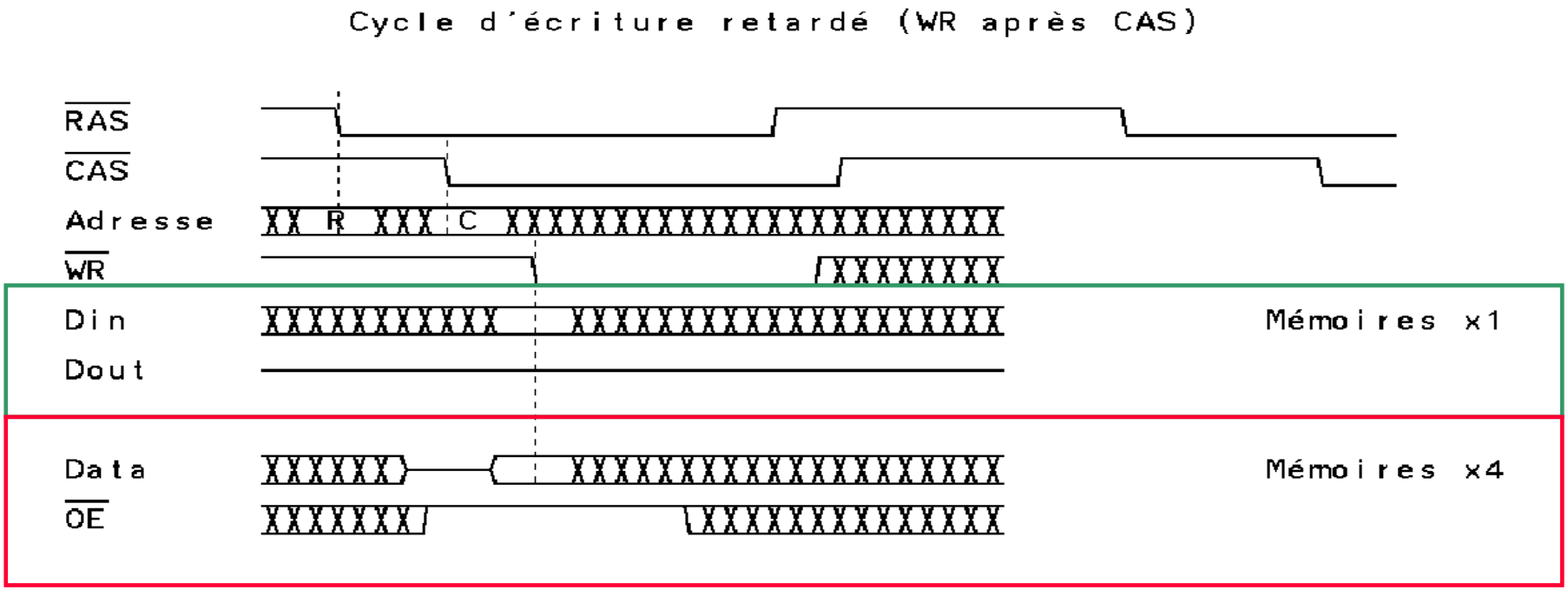
DRAM read access



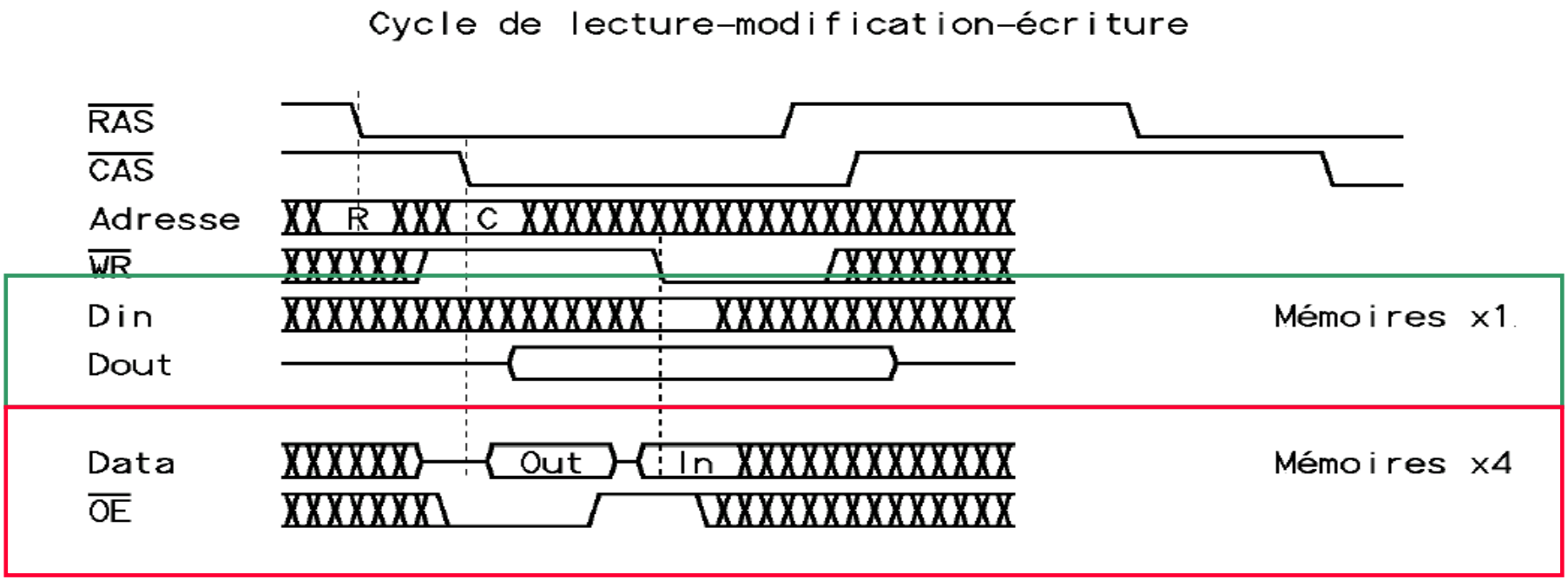
DRAM write access



DRAM late write



DRAM Read-Modify-Write



DRAM Precharge time

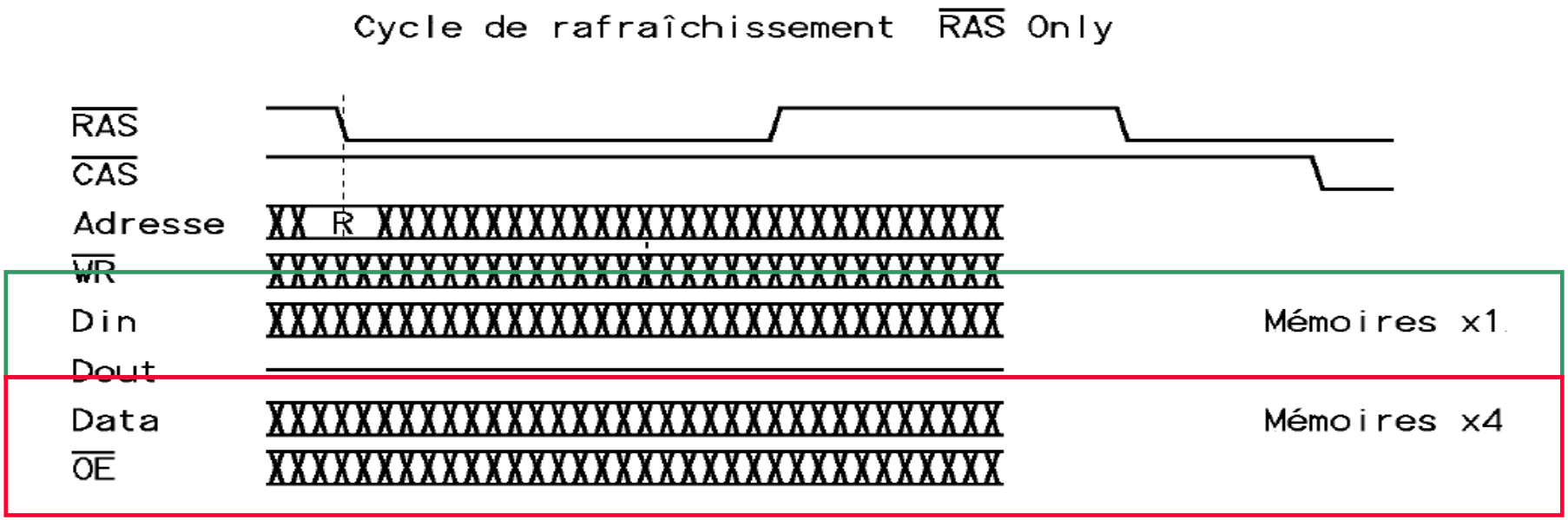
- Between 2 access there is the recovery time
- The vertical (column) lines are precharge to an intermediate voltage
- When access to the memory is done, the driver is less stressed to transfer the high/low logical level
- This take time !! ~30-50 ns

DRAM Refresh

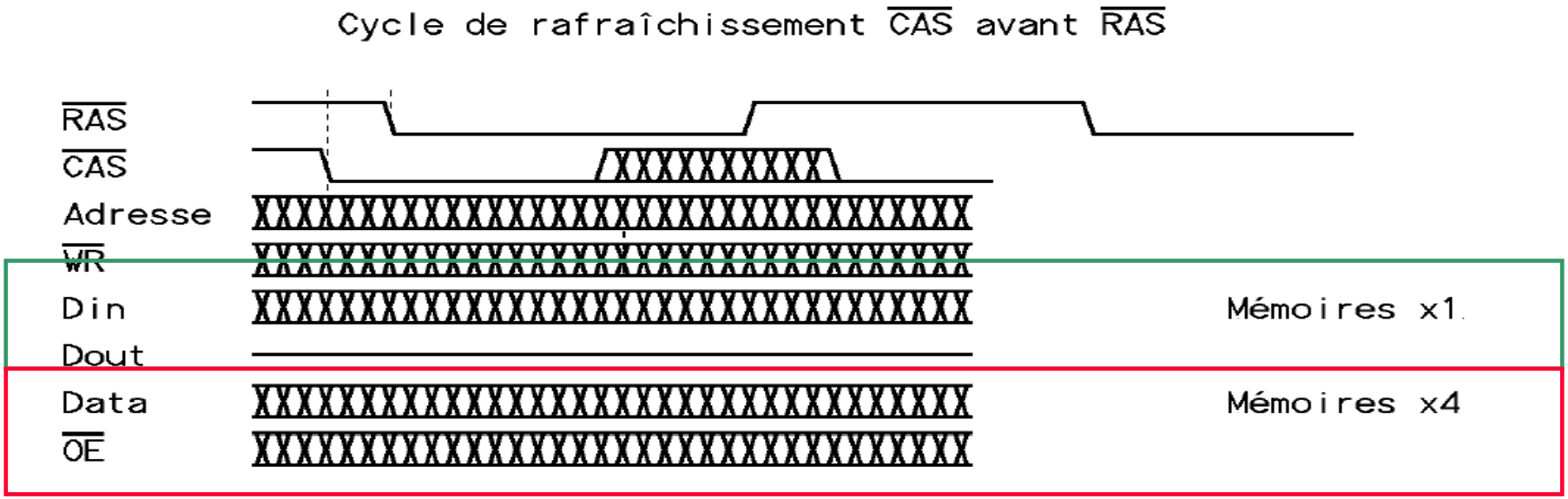
- The memory need to be refreshed to maintain its content

- Particular Cycles :
  - RAS only
  - CAS before RAS
  - Hidden refresh

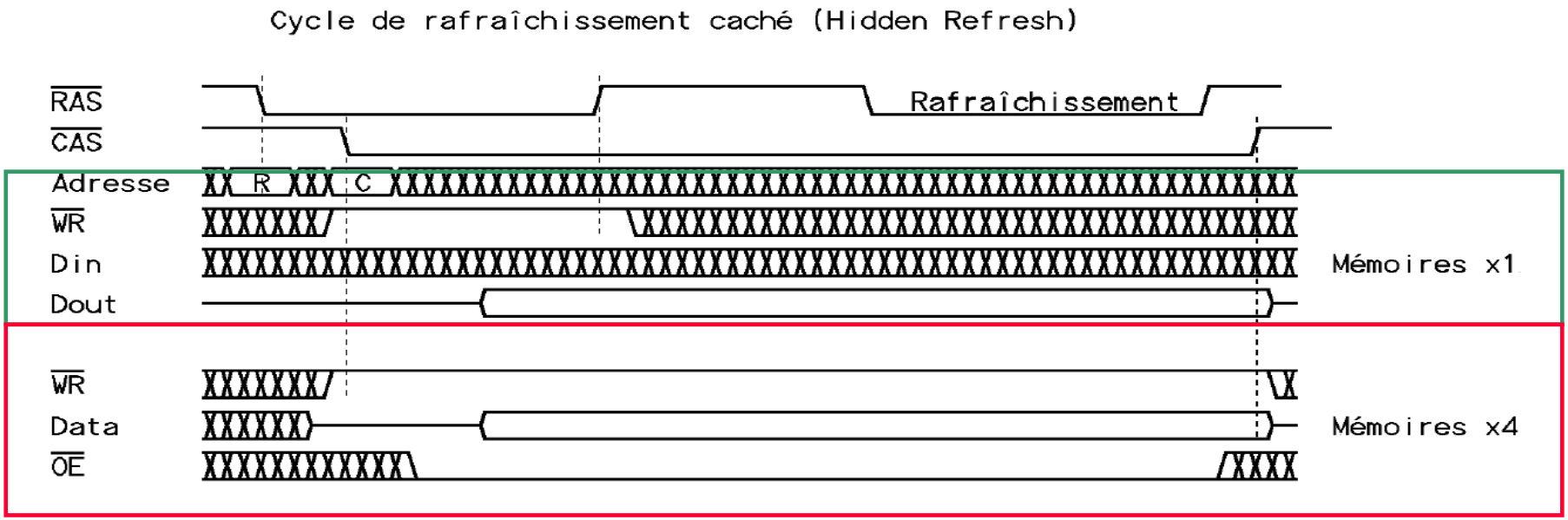
DRAM Refresh



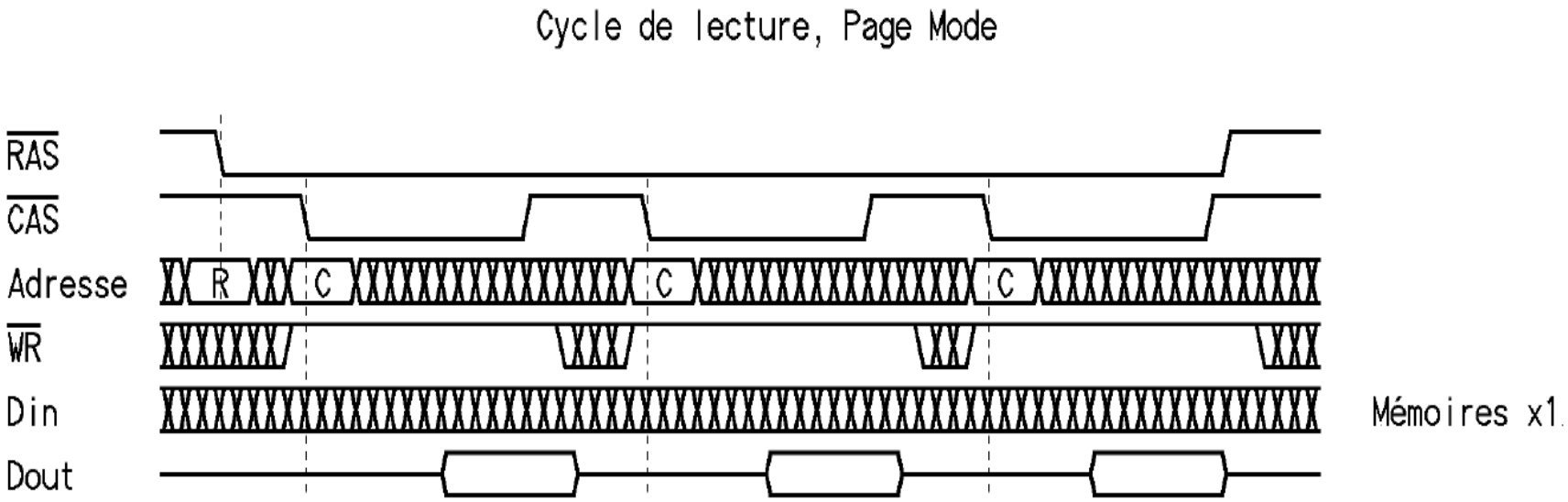
DRAM Refresh



DRAM Refresh

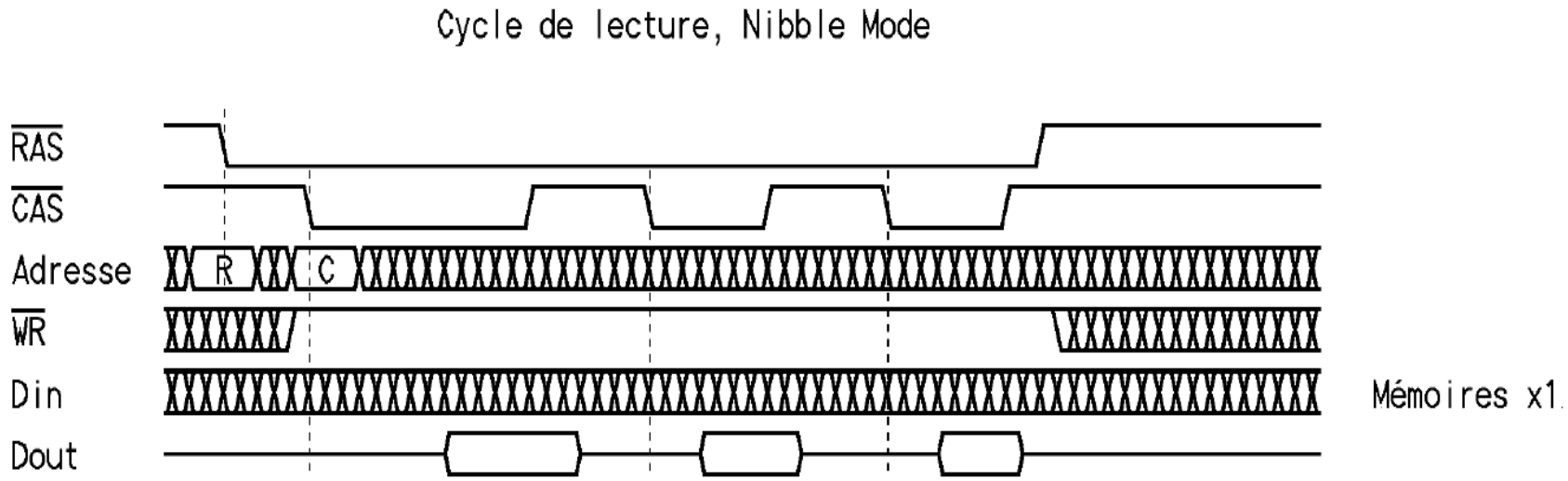


DRAM Accès multiples, page



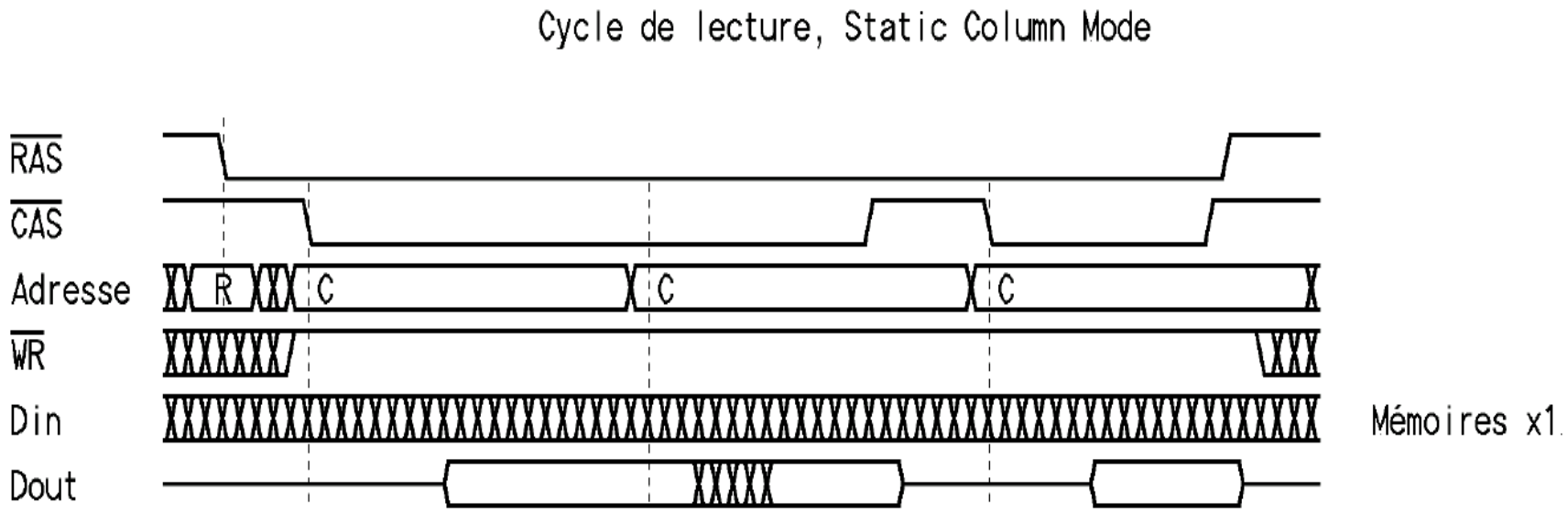
Page mode

DRAM Accès multiples, nibble



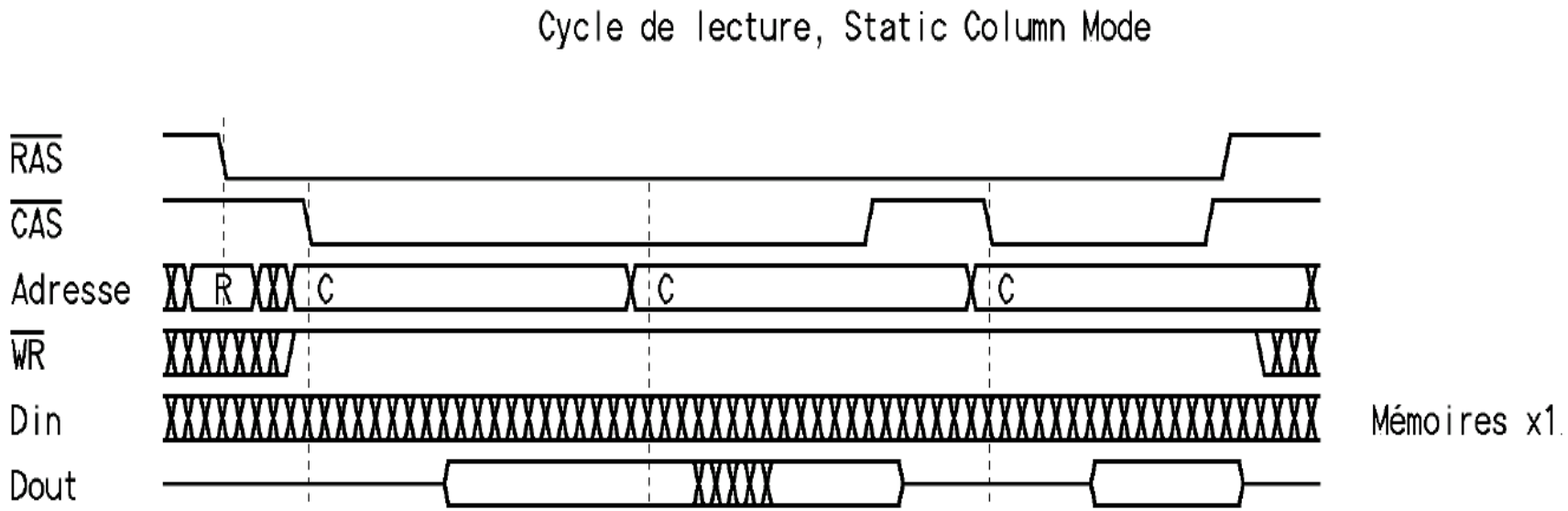
Nibble mode

DRAM Accès multiples, static column



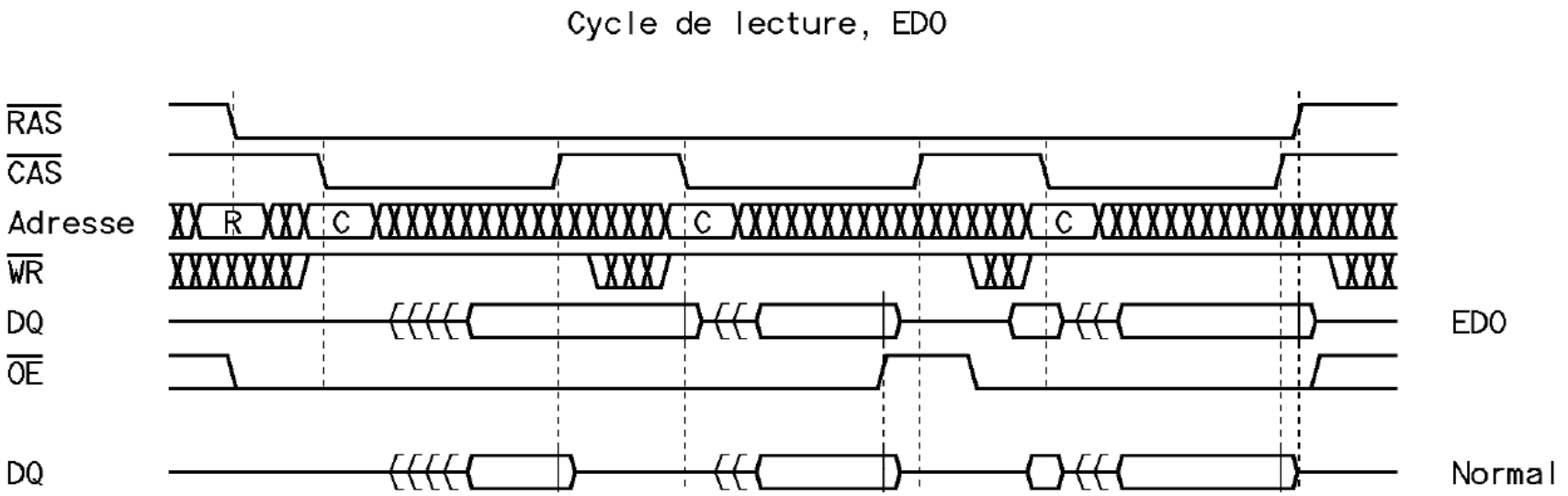
Static column mode

DRAM Accès multiples, static column



Static column mode

DRAM Accès multiples, EDO



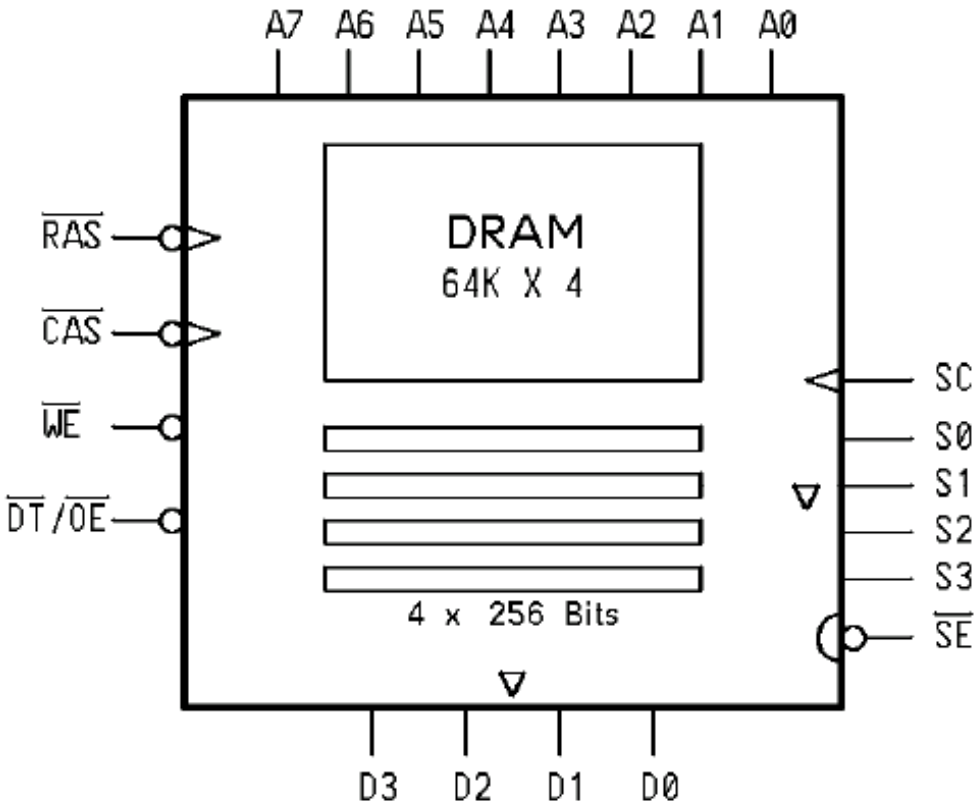
EDO

VRAM (Video RAM)

- Asynchronous Dynamic Memory
- Added "Serial Register"

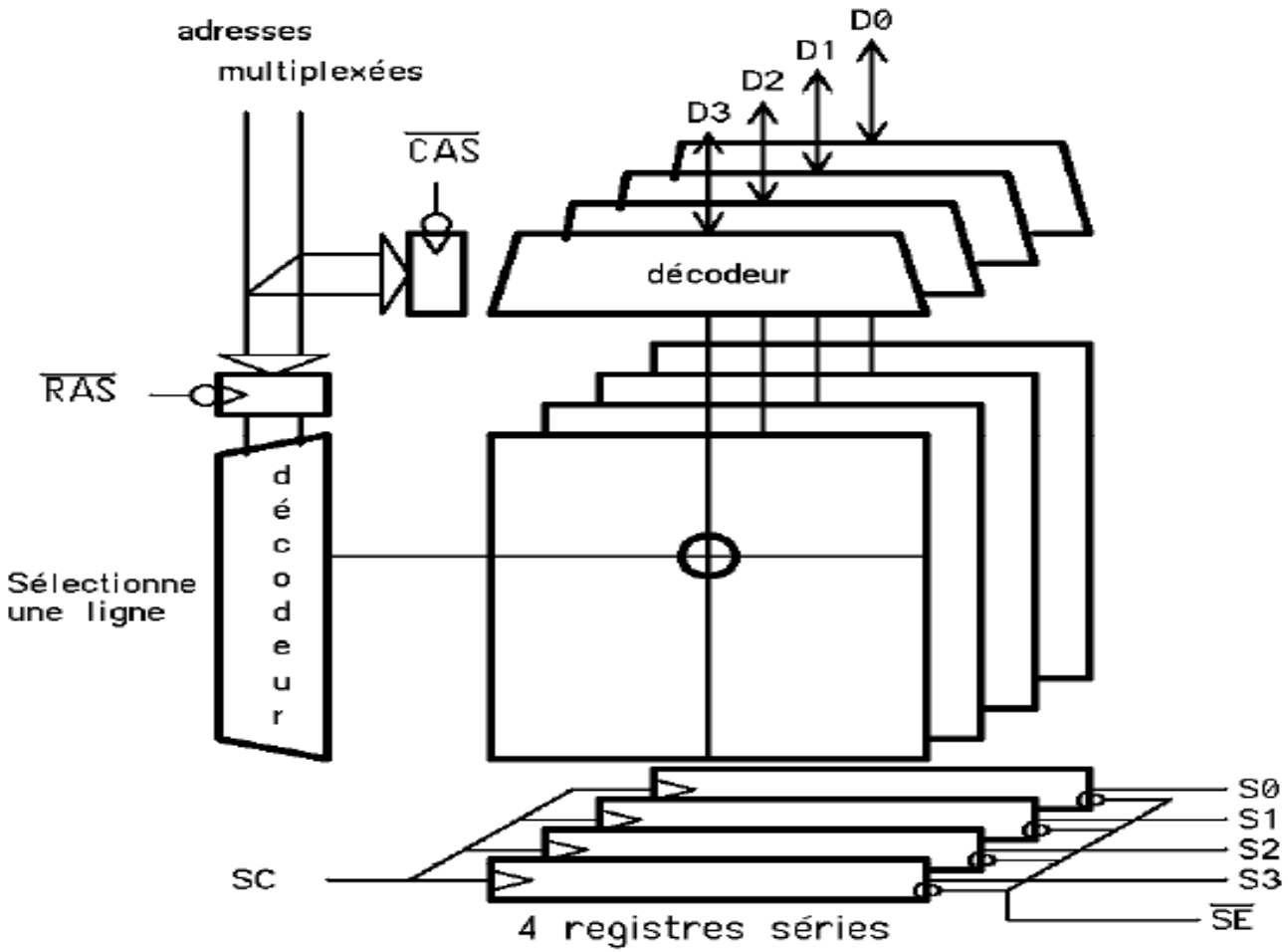
- Transfer between Dynamic array and serial line
- Independent serial transfers

VRAM (Video RAM)

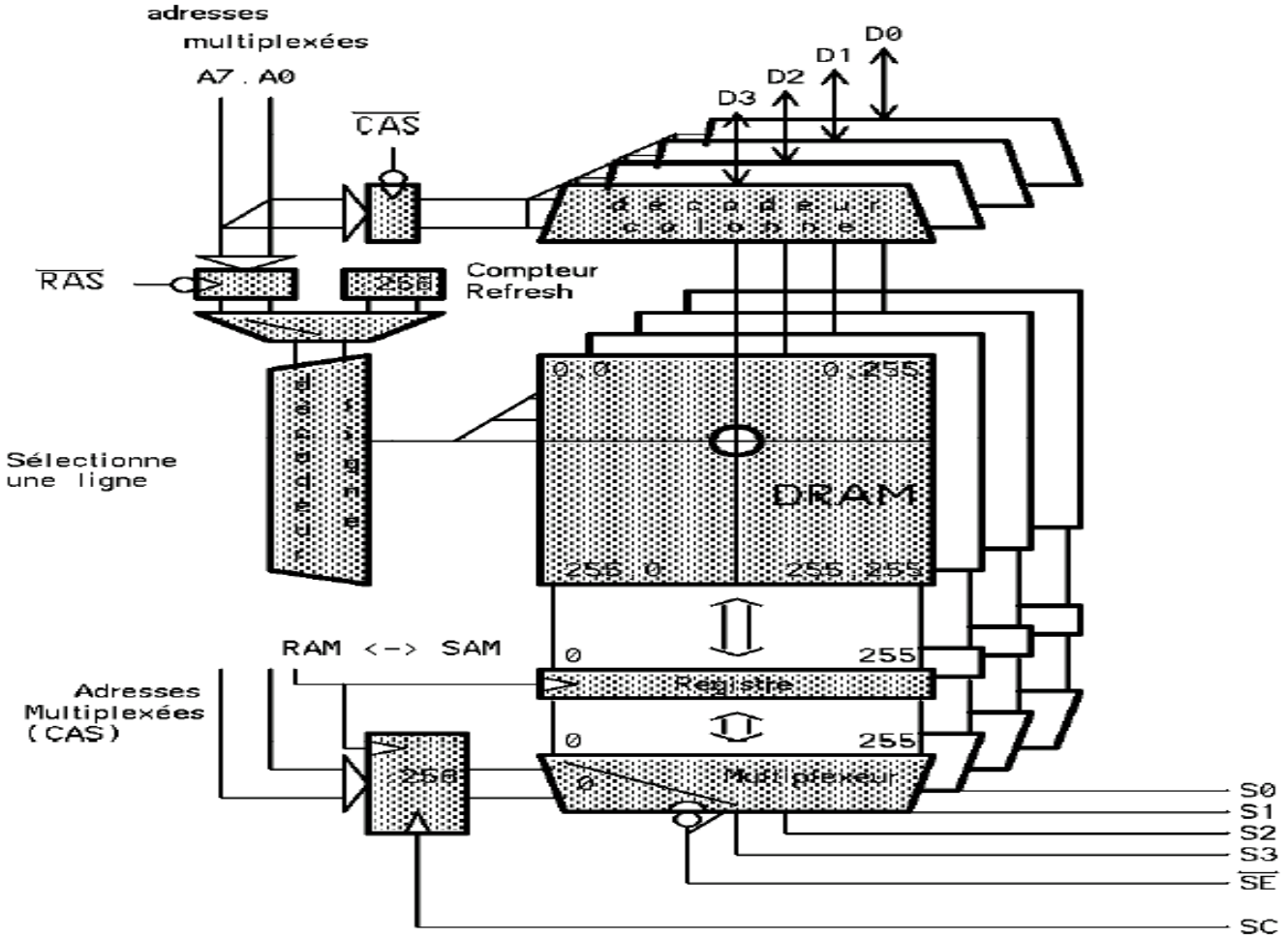


Ex: First VRAM 64k x 4,
4 serial bits

VRAM (Video RAM) simple model



VRAM parallel register+counter+mux



VRAM parallel register+counter+mux

- The serial register is build from a parallel register → the full content of the selected line (Row) is transferred in a large register
- During the column phase, the address is transferred in a counter: the start address of the line
- The counter select a multiplexer, thus the parallel register is transform in a serial register!

SDRAM

Synchronous Dynamic RAM

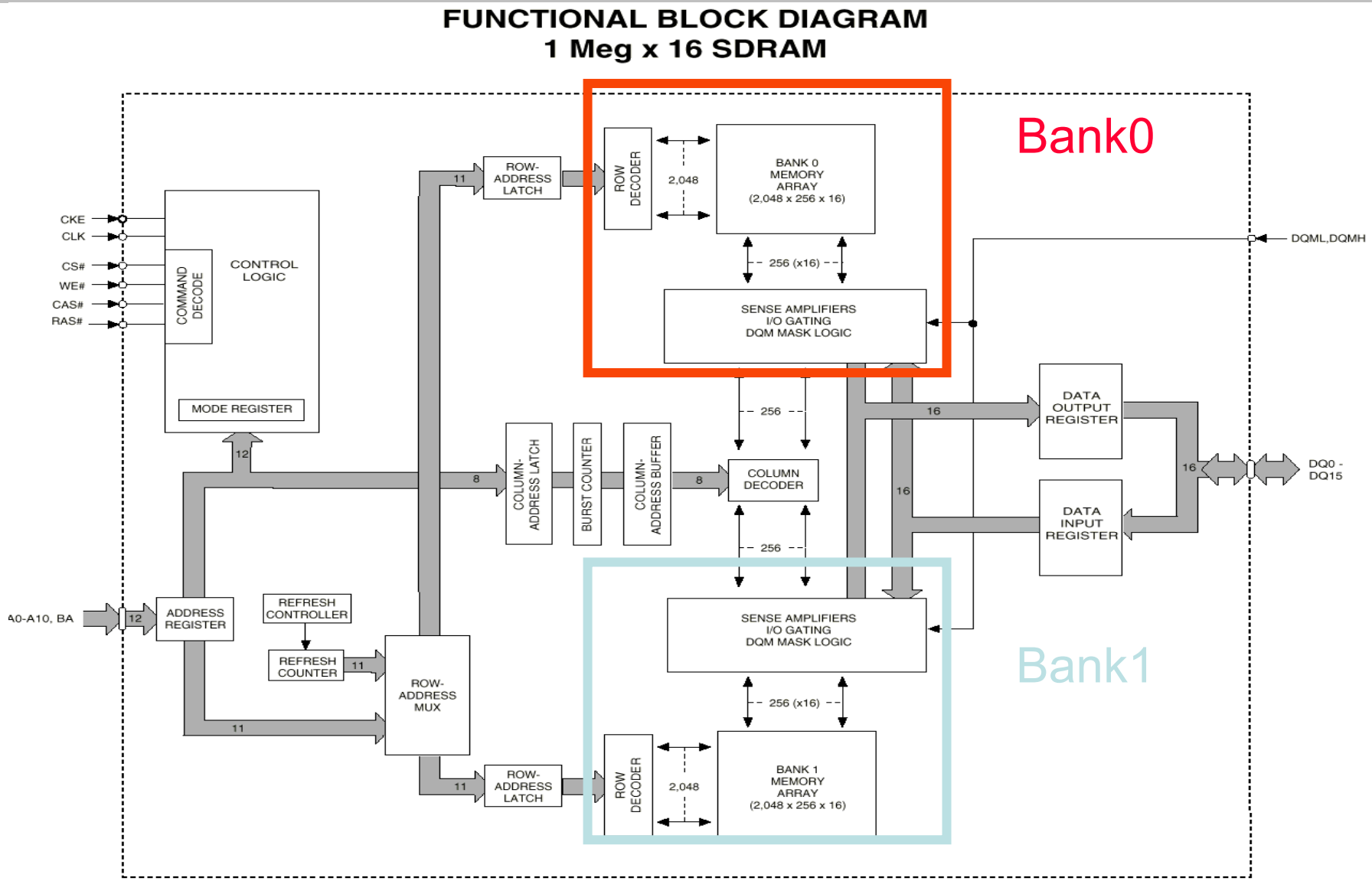
SDRAM (Synchronous DRAM)

- synchronous DRAM Memories
- 16 Mbits..256 Mbits
- x4, x8, x16, x32
- 3.3V, 2.5V → 1.8V
- Clk 200MHz
- 2 Banks / 4 Banks
- PC100 SDRAM standard
- Command ACTIVE to send with the Row and Bank address
- Read, Write Command with Column address
- Concurrent Precharge between 2 banks

SDRAM

- Clock to synchronized every signals
- Internal Pipeline
- New column address possible in every transfer cycle
- Internal banks available to shadow the precharge
- Self-refresh (Self-Refresh command)

SDRAM


FUNCTIONAL BLOCK DIAGRAM
1 Meg x 16 SDRAM
Bank0
Bank1
CKE
CLK
CS#
WE#
CAS#
RAS#
COMMAND DECODE
CONTROL LOGIC
MODE REGISTER
ROW-ADDRESS LATCH
ROW DECODER
2,048
BANK 0 MEMORY ARRAY (2,048 x 256 x 16)
256 (x16)
SENSE AMPLIFIERS I/O GATING DQM MASK LOGIC
DQML,DQMH
DATA OUTPUT REGISTER
DATA INPUT REGISTER
DQ0 - DQ15
COLUMN-ADDRESS LATCH
BURST COUNTER
COLUMN-ADDRESS BUFFER
COLUMN DECODER
256
A0-A10, BA
ADDRESS REGISTER
REFRESH CONTROLLER
REFRESH COUNTER
ROW-ADDRESS MUX
BANK 1 MEMORY ARRAY (2,048 x 256 x 16)
11
12
8
16

SDRAM

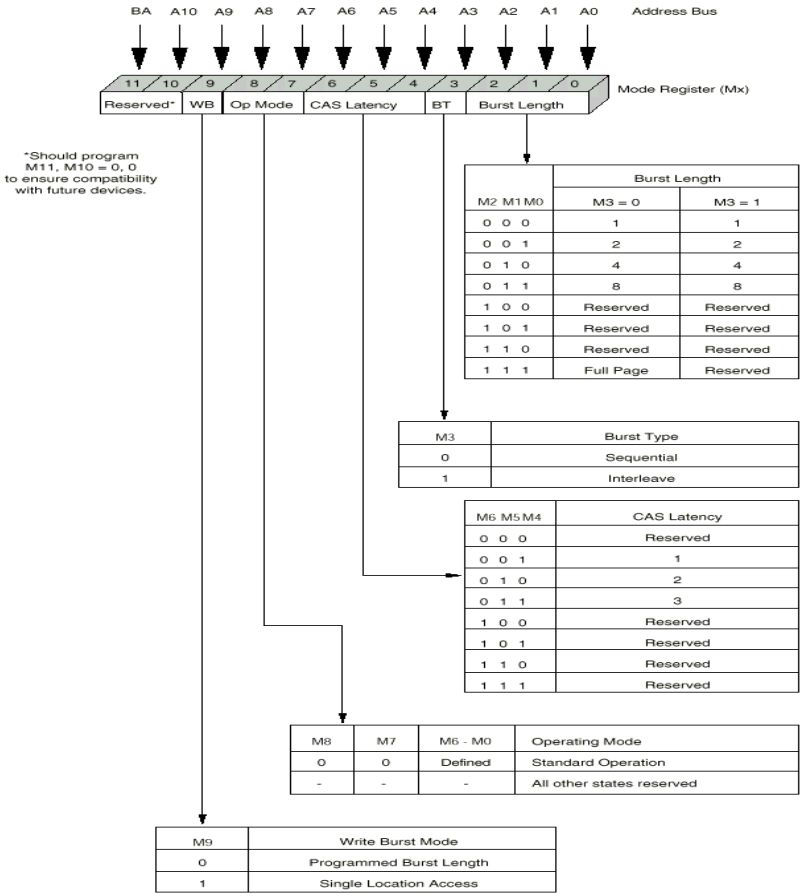


Figure 1
MODE REGISTER DEFINITION

BURST DEFINITION

Burst Length	Starting Column Address:	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n = A0-A7 (location 0-255)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... …Cn-1, Cn…	Not supported

SDRAM

TRUTH TABLE 1 – Commands and DQM Operation
(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column and start READ burst)	L	H	L	H	X	Bank/Col	X	4
WRITE (Select bank and column and start WRITE burst)	L	H	L	L	X	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	OpCode	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

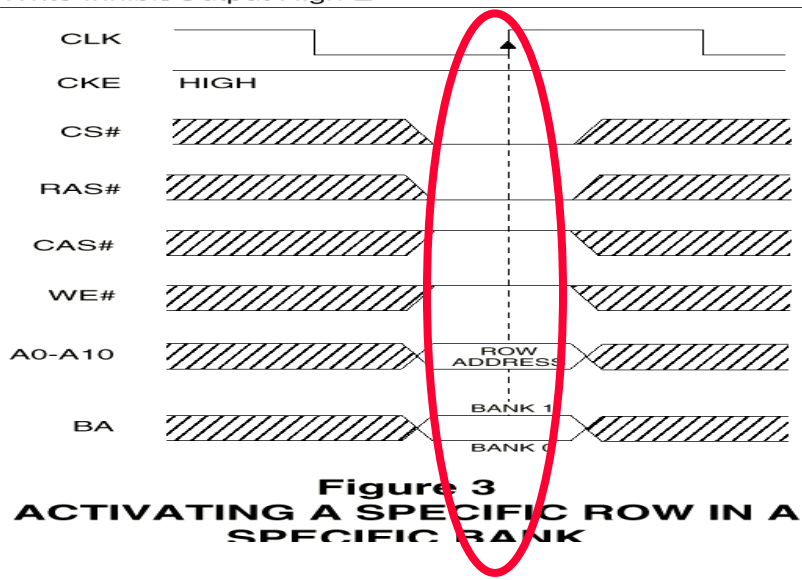
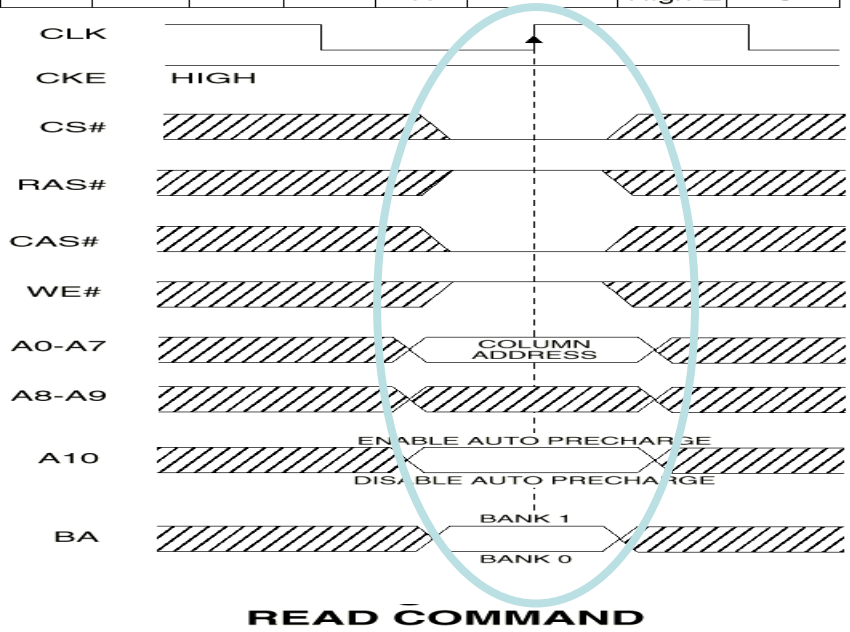
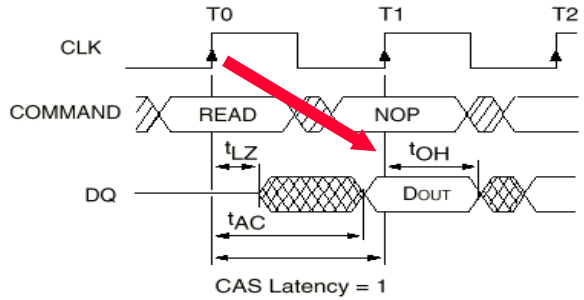


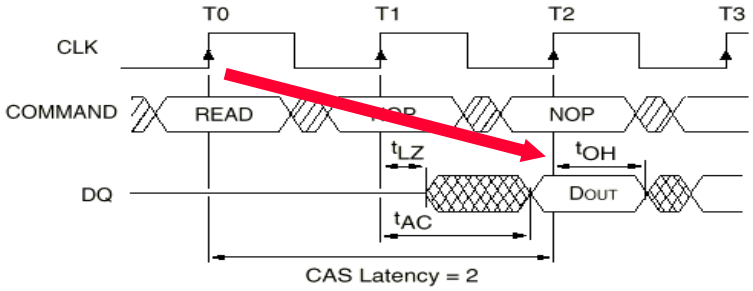
Figure 3
ACTIVATING A SPECIFIC ROW IN A SPECIFIC BANK

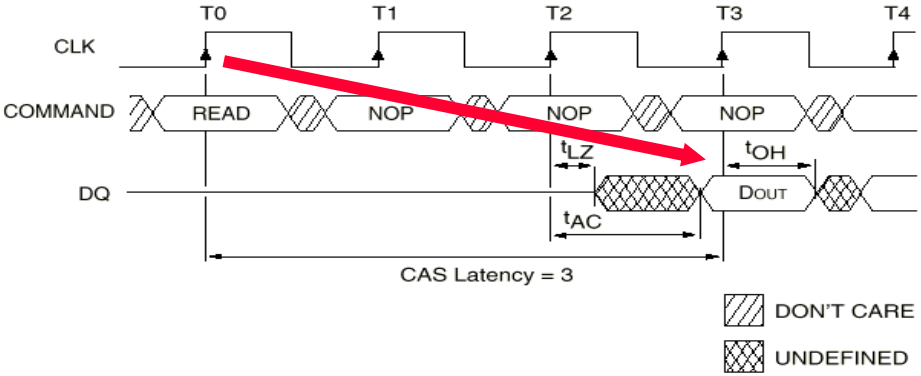


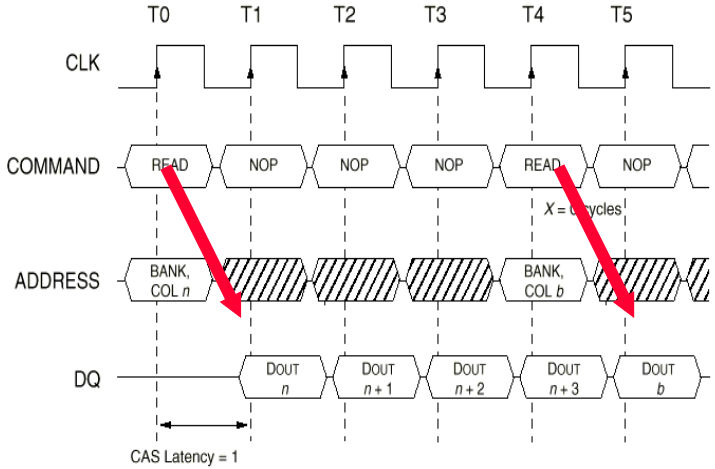
READ COMMAND

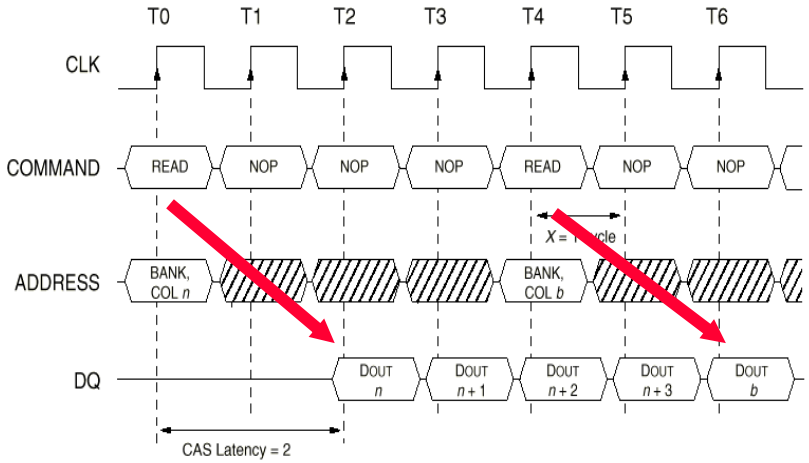
SDRAM Cas Latency (CL) Read cycle





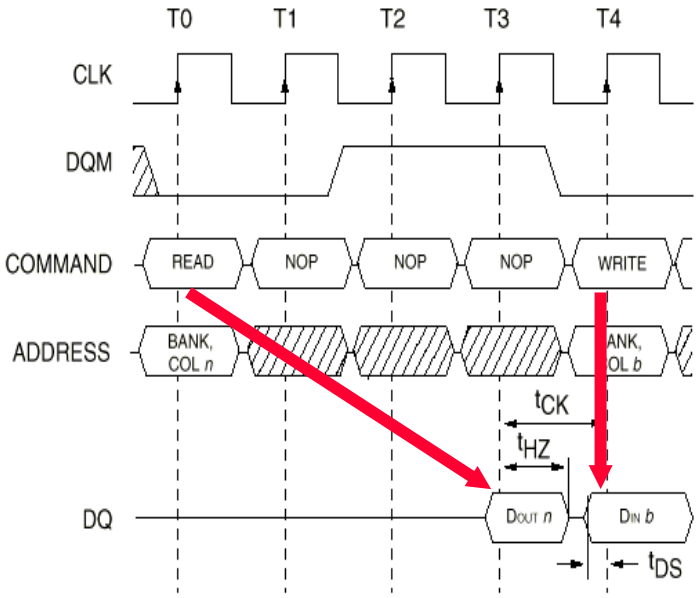






4 burst accesses

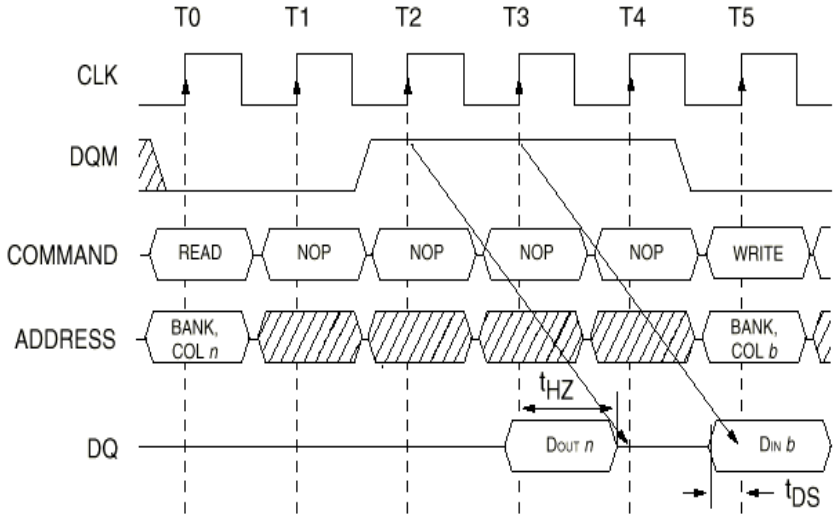
SDRAM Write data with command



NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

CL=3

READ TO WRITE

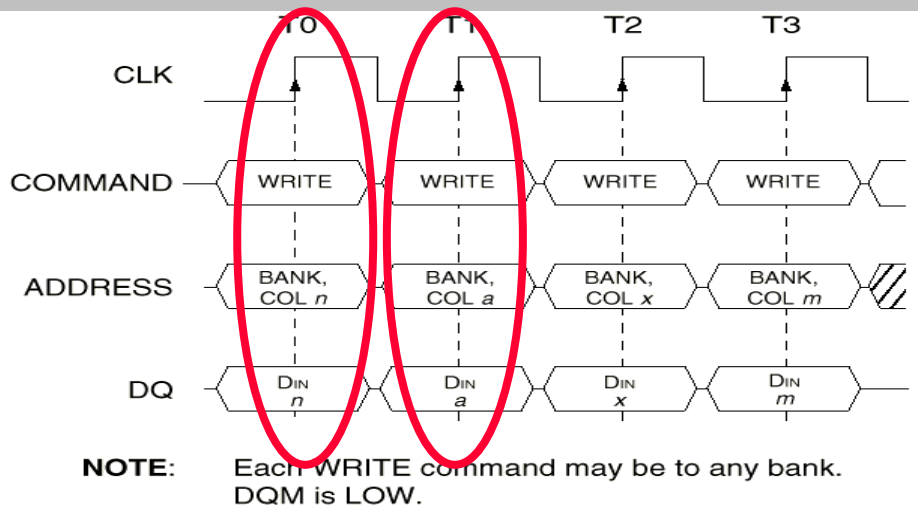


NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank.

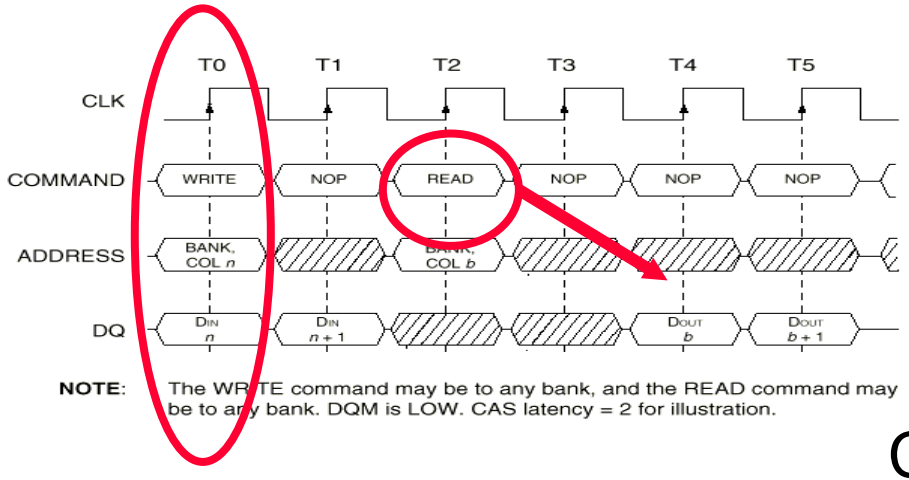
DON'T CARE

READ TO WRITE WITH EXTRA CLOCK CYCLE

SDRAM



RANDOM WRITE CYCLES



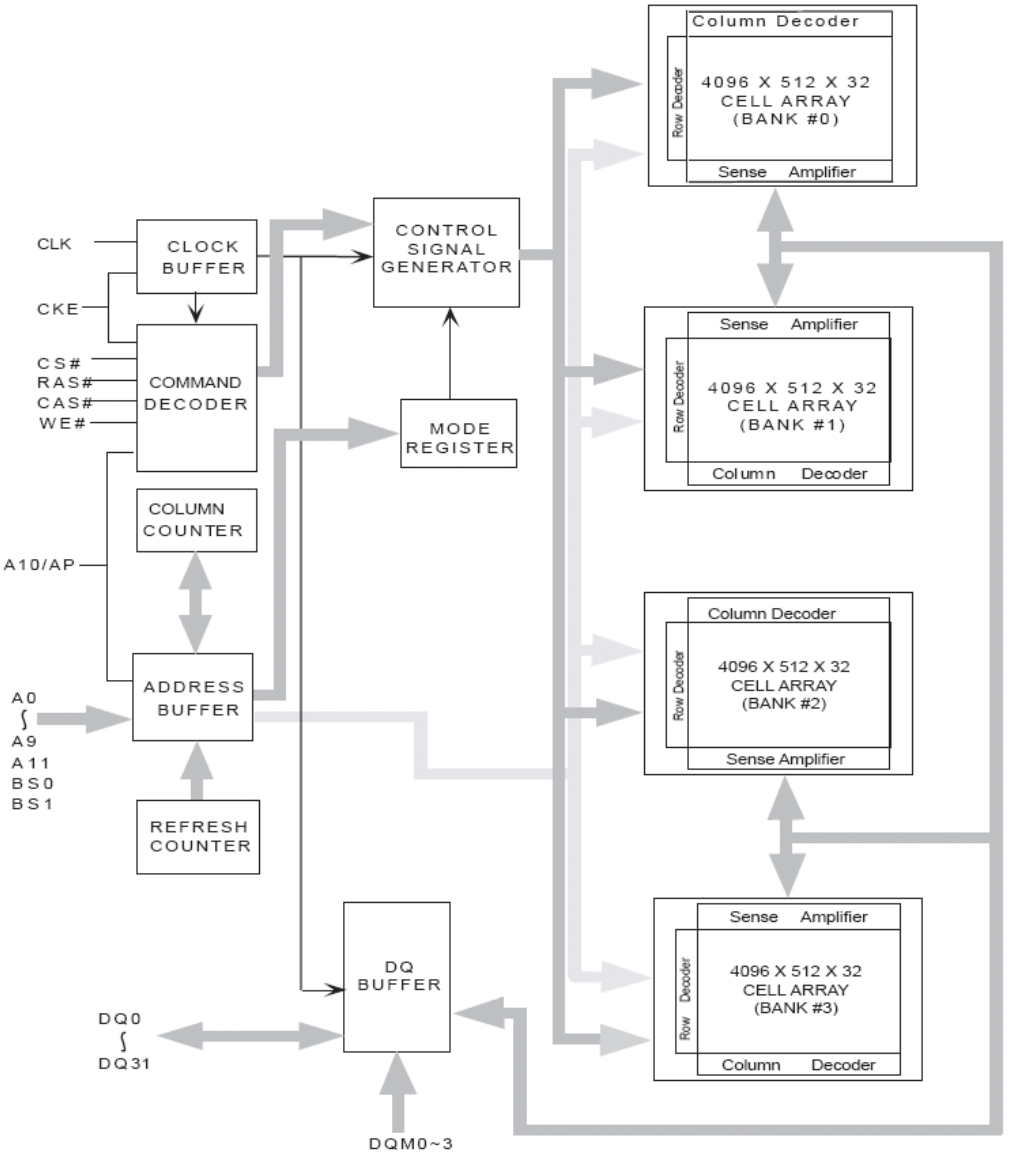
CL=2

WRITE TO READ

SDRAM 4 banks ex: IS42S32800B

- Nb row (12) ≠
  Nb Column(9)

- 4 banks
- x32 bits width (4x8bits)
- 256 Mbits :
  - 4 x 2M x 32
- Masked by DQM<3..0>



SDRAM 4 banks ex: IS42S32800B

See the full documentation

For all specific timings relationships

http://www.issi.com/pdf/42S32800B.pdf

Command	State	CKEn-1	CKE	DQM(6)	BS0,1	A10	A11,A9-0	CS#	RAS#	CAS#	WE#
BankActivate	Idle (3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active (3)	H	X	X	V	L	Column address (A0 ~A7)	L	H	L	L
Write and Auto Precharge	Active (3)	H	X	X	V	H		L	H	L	L
Read	Active (3)	H	X	X	V	L	Column address (A0 ~A7)	L	H	L	H
Read and Autoprecharge	Active (3)	H	X	X	V	H		L	H	L	H
Mode Register	Set Idle	H	X	X		OP code		L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	H	X	X	X
	(SelfRefresh)							L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any	L	H	X	X	X	X	H	X	X	X
	(PowerDown)							L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Note:

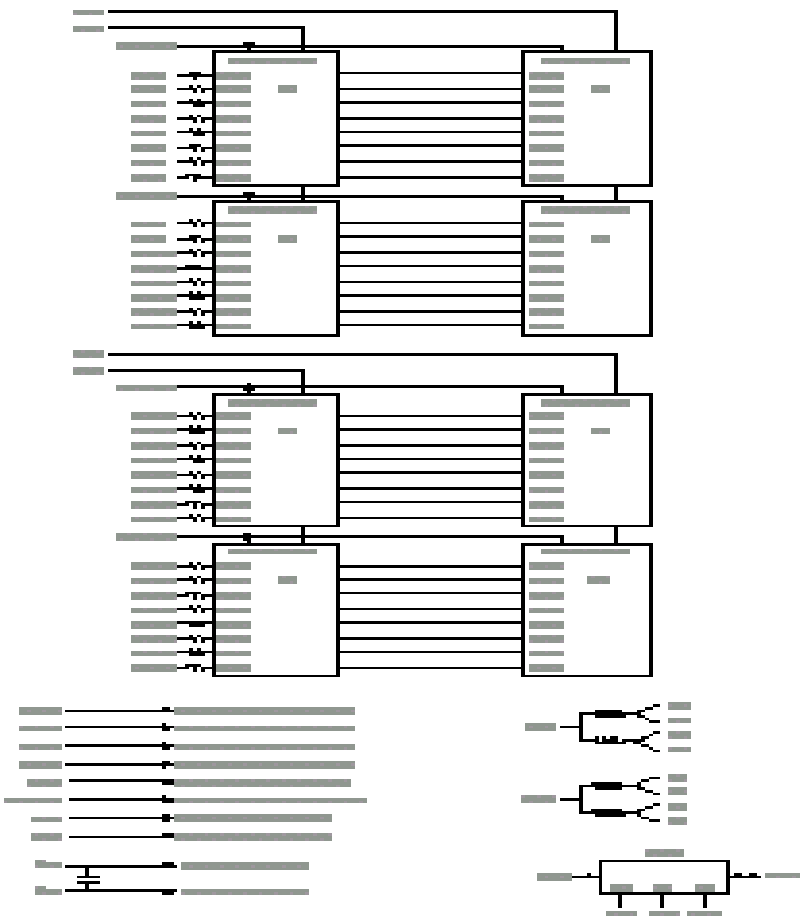
1. V =Valid,X =Don 't care,L =Logic low,H =Logic high
2. CKEn signal is input level when commands are provided.
   CKEn-1 signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BS signal.
4. Device state is 1,2,4,8,and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
   When this command is asserted in the burst cycle,device state is clock suspend mode.
6. DQM0-3

Module DIMM SDRAM

- Module DIMM 100-Pin
- Bus x32
- Synchronous
- SDRAM Memory

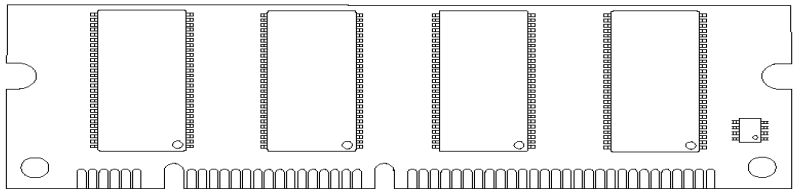
SDRAM (x32, x36)

FUNCTIONAL BLOCK DIAGRAM
MT8LSDT1632U (64MB)



PIN ASSIGNMENT (Front View)

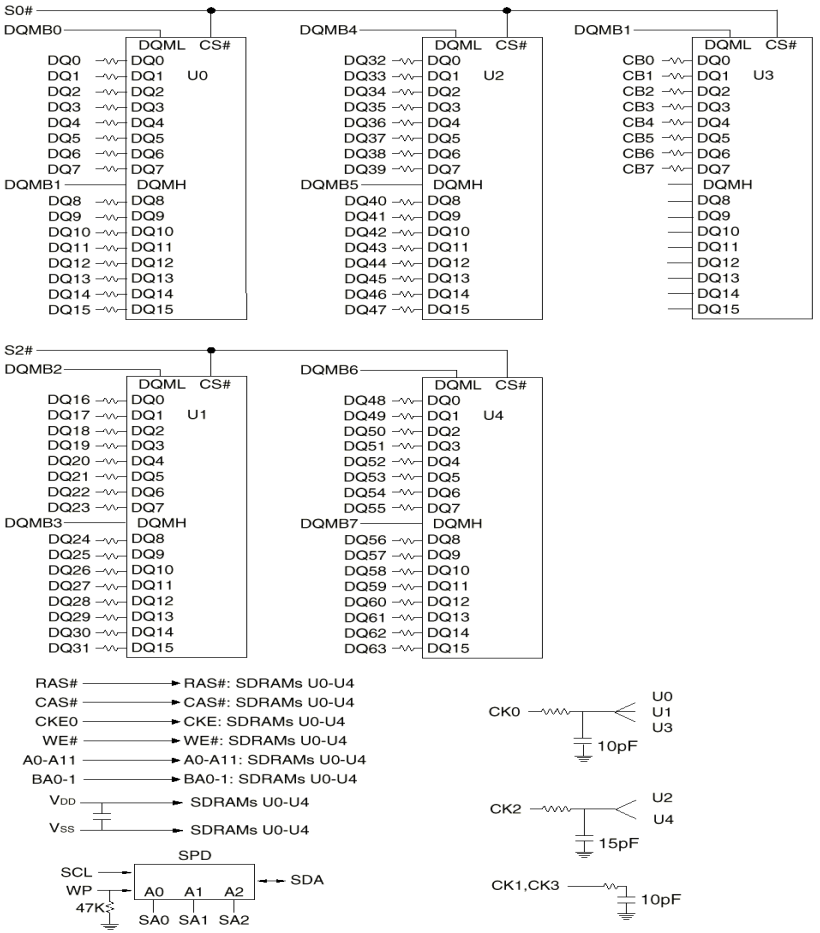
100-Pin DIMM



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	Vss	26	Vss	51	Vss	76	Vss
2	DQ0	27	CKE0	52	DQ8	77	CKE1
3	DQ1	28	WE#	53	DQ9	78	DNU
4	DQ2	29	S0#	54	DQ10	79	S1#
5	DQ3	30	S2#	55	DQ11	80	S3#
6	VDD	31	VDD	56	VDD	81	VDD
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQMB0	36	Vss	61	DQMB1	86	Vss
12	Vss	37	DQMB2	62	Vss	87	DQMB3
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	VDD	67	A9	92	VDD
18	A10	43	DQ20	68	BA0	93	DQ28
19	BA1	44	DQ21	69	A11	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	VDD	46	DQ23	71	VDD	96	DQ31
22	DNU	47	Vss	72	RAS#	97	Vss
23	RFU	48	SDA	73	CAS#	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	CK0	50	VDD	75	CK1	100	SA2

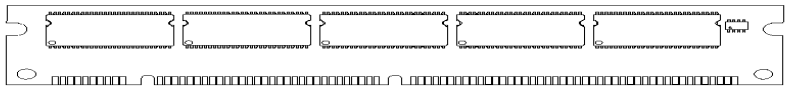
SDRAM (x64, x72)

FUNCTIONAL BLOCK DIAGRAM
MT5LSDT472A (32MB)



PIN ASSIGNMENT (Front View)

168-Pin DIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	NC (S3#)
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	NC (A13)
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC (CKE1)	105	CB4	147	NC
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	NC (S1#)	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	NC (CK3)
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	NC/WP*	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	NC (CK1)	167	SA2
42	CK0	84	VDD	126	NC (A12)	168	VDD

*WP applies to -10B/-10C versions only

PC100 SDRAM DIMM Dual In Line Memory module

- Specification from Intel for DIMM 100MHz
- EEPROM memory on the module for the specification of the DIMM

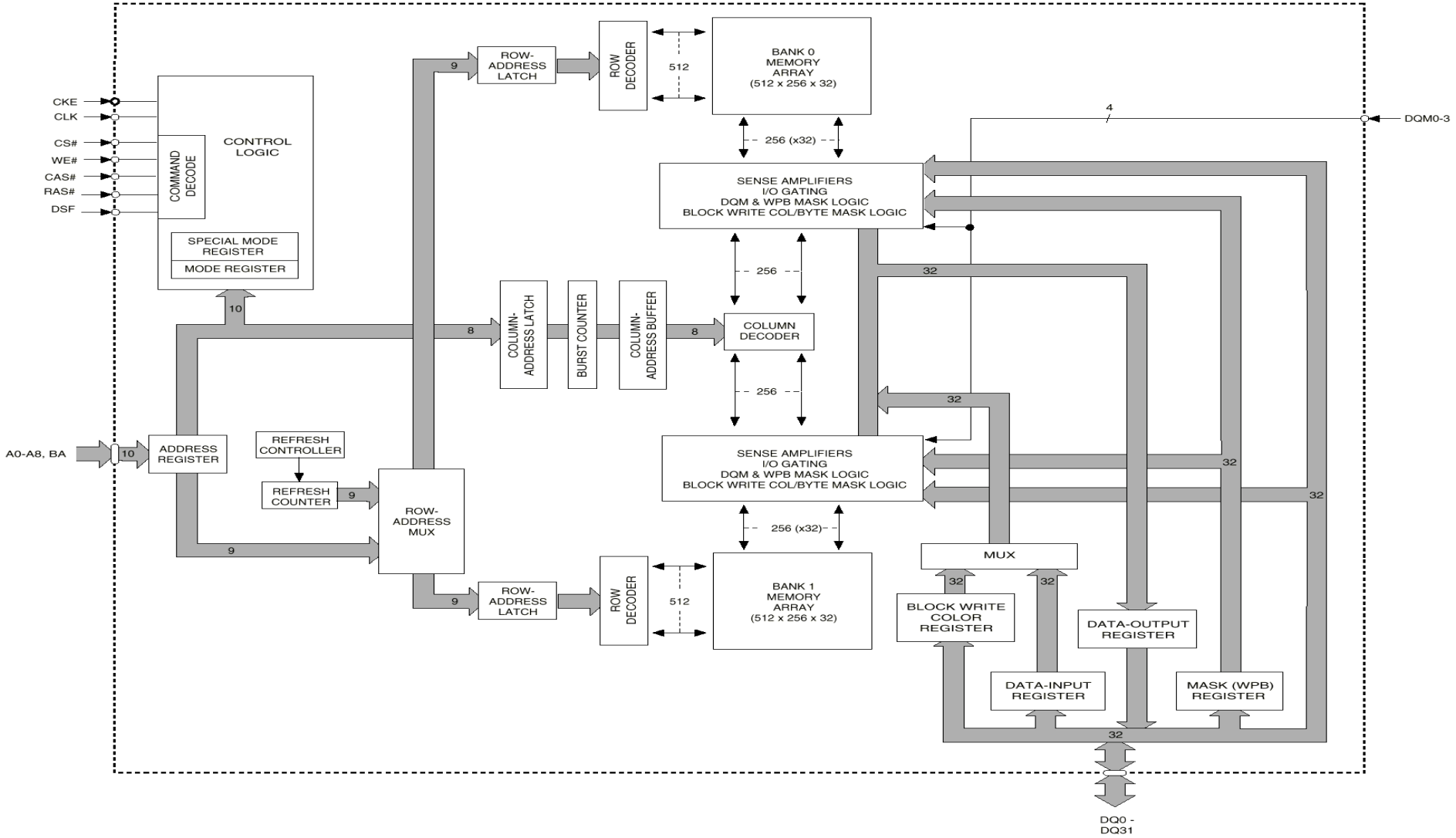
  → SPD : Serial Presence detect
- Specification for memory from 64Mbytes to 1024 Mbytes (1GBytes)
- Module without buffer
- Module with register to be used with up to 36 chips

- Old specification (historical)

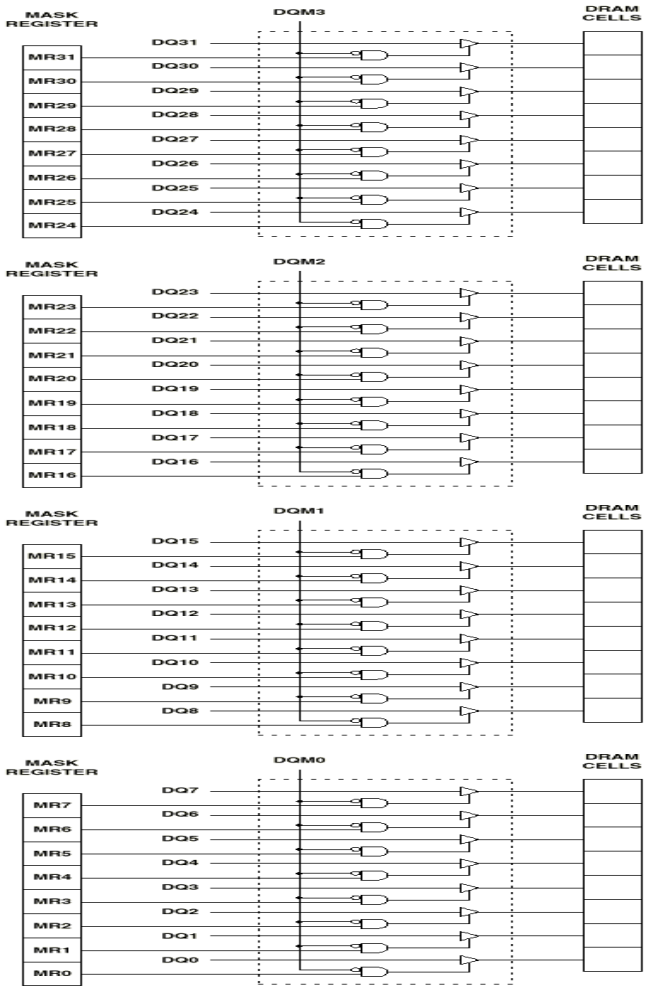
SGRAM Synchronous Graphic RAM

- 128kx32, 256kx32, 512kx32
- Synchronous
- Double banque
- Burst 1, 2, 4, 8 ou pleine page
- Block Write, Write par bit
- Auto precharge, auto refresh
- 3.3V

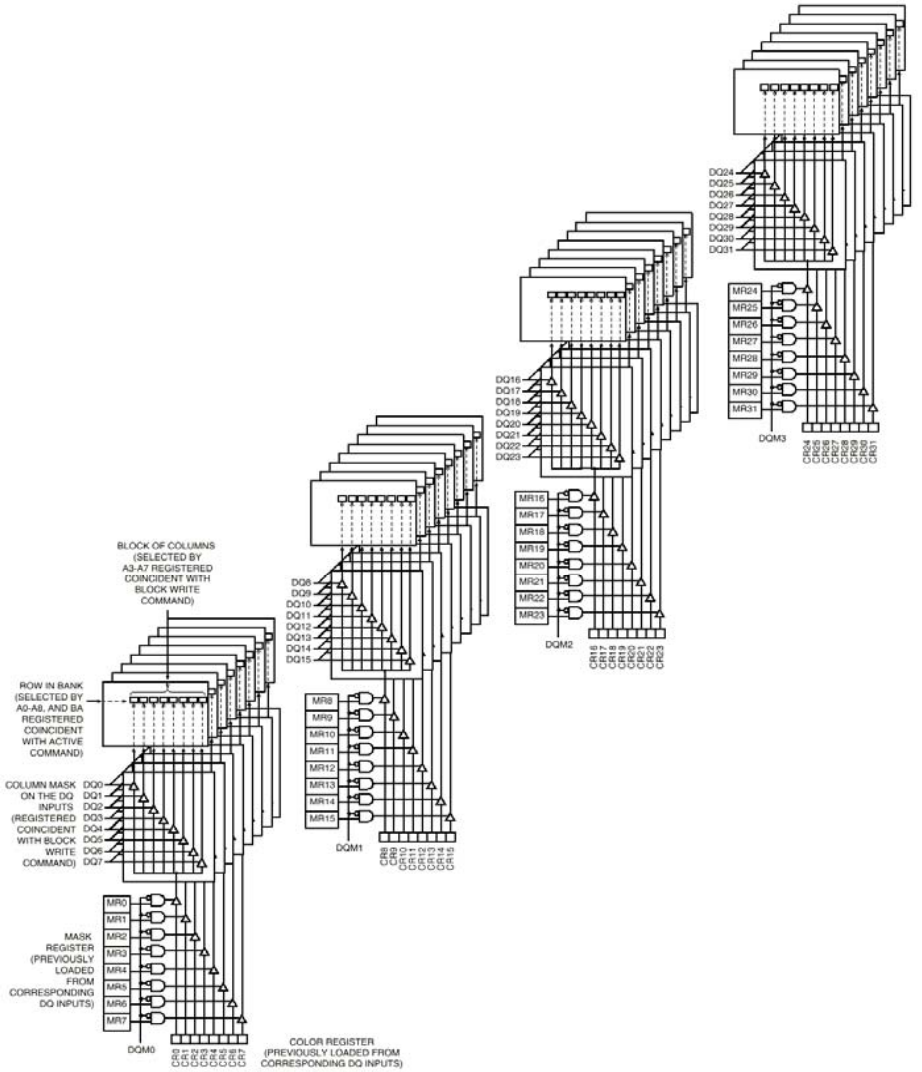
SGRAM Synchronous Graphic RAM



SGRAM



WRITE MASKING – FUNCTIONAL REPRESENTATION



BLOCK WRITE MASKING – FUNCTIONAL REPRESENTATION

SGRAM

CURRENT STATE	CS#	RAS#	CAS#	WE#	DSF	COMMAND (ACTION)
Any	H	X	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)
	L	H	H	H	L	NO OPERATION (NOP/Continue previous operation)
Idle	L	L	H	H	L	ACTIVE (Select bank and activate row)
	L	L	H	H	H	ACTIVE w/WPB (Select bank, activate row and WPB)
	L	L	L	H	L	AUTO REFRESH
	L	L	L	L	L	LOAD MODE REGISTER
	L	L	L	L	H	LOAD SPECIAL MODE REGISTER
	L	L	H	L	L	PRECHARGE
Row Active	L	H	L	H	L	READ (Select bank and column and start READ burst)
	L	H	L	L	L	WRITE (Select bank and column and start WRITE burst)
	L	H	L	L	H	BLOCK WRITE (Select bank and column and start block write access)
	L	L	H	L	L	PRECHARGE (Deactivate row in bank or banks)
	L	L	L	L	H	LOAD SPECIAL MODE REGISTER
Read (Auto-Precharge Disabled)	L	H	L	H	L	READ (Select bank and column and start new READ burst)
	L	H	L	L	L	WRITE (Select bank and column and start WRITE burst)
	L	H	L	L	H	BLOCK WRITE (Select bank and column and start block write access)
	L	L	H	L	L	PRECHARGE (Truncate READ burst, start PRECHARGE)
	L	H	H	L	L	BURST TERMINATE
Write (Auto-Precharge Disabled)	L	H	L	H	L	READ (Select bank and column and start READ burst)
	L	H	L	L	L	WRITE (Select bank and column and start new WRITE burst)
	L	H	L	L	H	BLOCK WRITE (Select bank and column and start block write access)
	L	L	H	L	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)
	L	H	H	L	L	BURST TERMINATE

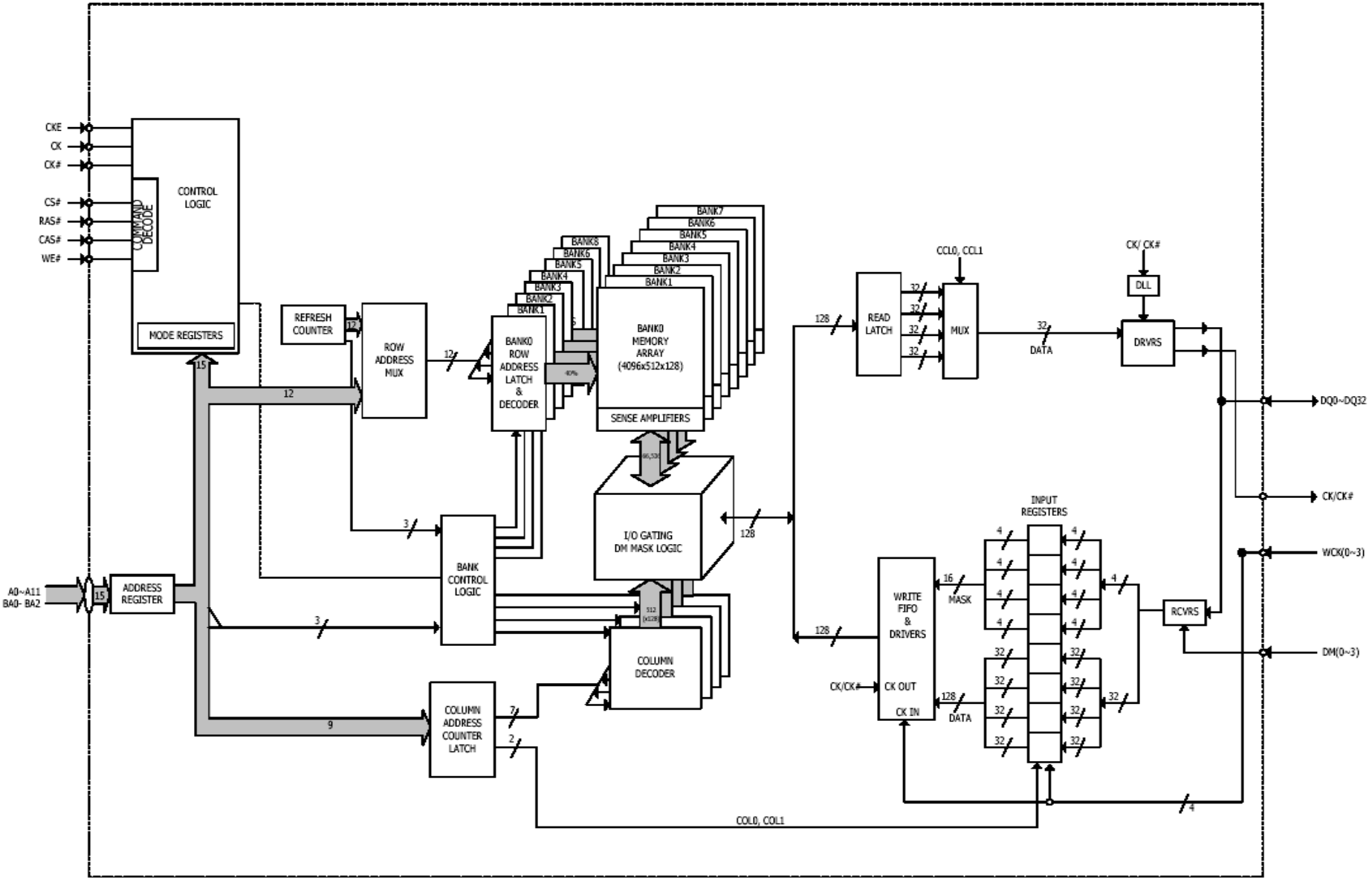
Graphics Memory GDDR

- **Features**
  - 2.2V +/-0.1V VDD/VDDQ power supply supports 900 / 800MHz
  - 2.0V VDD/ VDDQ wide range min/max power supply supports 700MHz
  - 1.8V VDD/ VDDQ wide range min/max power supply supports 500 / 600MHz
  - Single ended READ Strobe (RDQS) per byte
  - Single ended WRITE Strobe (WDQS) per byte
  - Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
  - Calibrated output driver
  - Differential clock inputs (CK and CK#)
  - Commands entered on each positive CK edge
  - RDQS edge-aligned with data for READ; with WDQScenter-aligned with data for WRITE
  - Eight internal banks for concurrent operation
  - Data mask (DM) for masking WRITE data

Graphics Memory GDDR

- **Features**
  - 4n prefetch
  - Programmable burst lengths: 4, 8
  - 32ms, 8K-cycle auto refresh
  - Auto precharge option
  - Auto Refresh and Self Refresh Modes
  - 1.8V Pseudo Open Drain I/O
  - Concurrent Auto Precharge support
  - tRAS lockout support, Active Termination support
  - Programmable Write latency(1, 2, 3, 4, 5, 6)
  - Boundary Scan Feature for connectivity test(refer to JEDEC std., not in this version of Specifications)

Graphics Memory



DDR Dual Data Rate

- DDR-I
  PC1600 = DDR 200MHz Data-rate (100 Clk x 2) 1.6Gb/Sec
  PC2100 = DDR 266MHz Data-rate (133 Clk x 2) 2.1Gb/Sec
  PC2400 = DDR 300MHz Date-rate (150 Clk x 2) 2.4Gb/Sec
  PC2700 = DDR 333MHz Data-rate (166 Clk x 2) 2.7Gb/Sec
  PC3000 = DDR 366MHz Data-rate (183 Clk x 2) 3.0Gb/Sec
  PC3200 = DDR 400MHz Data-rate (200 Clk x 2) 3.2Gb/Sec

  DDR-II
  PC4300 = DDR 533MHz Data-rate (266 Clk x 2) 4.3Gb/Sec

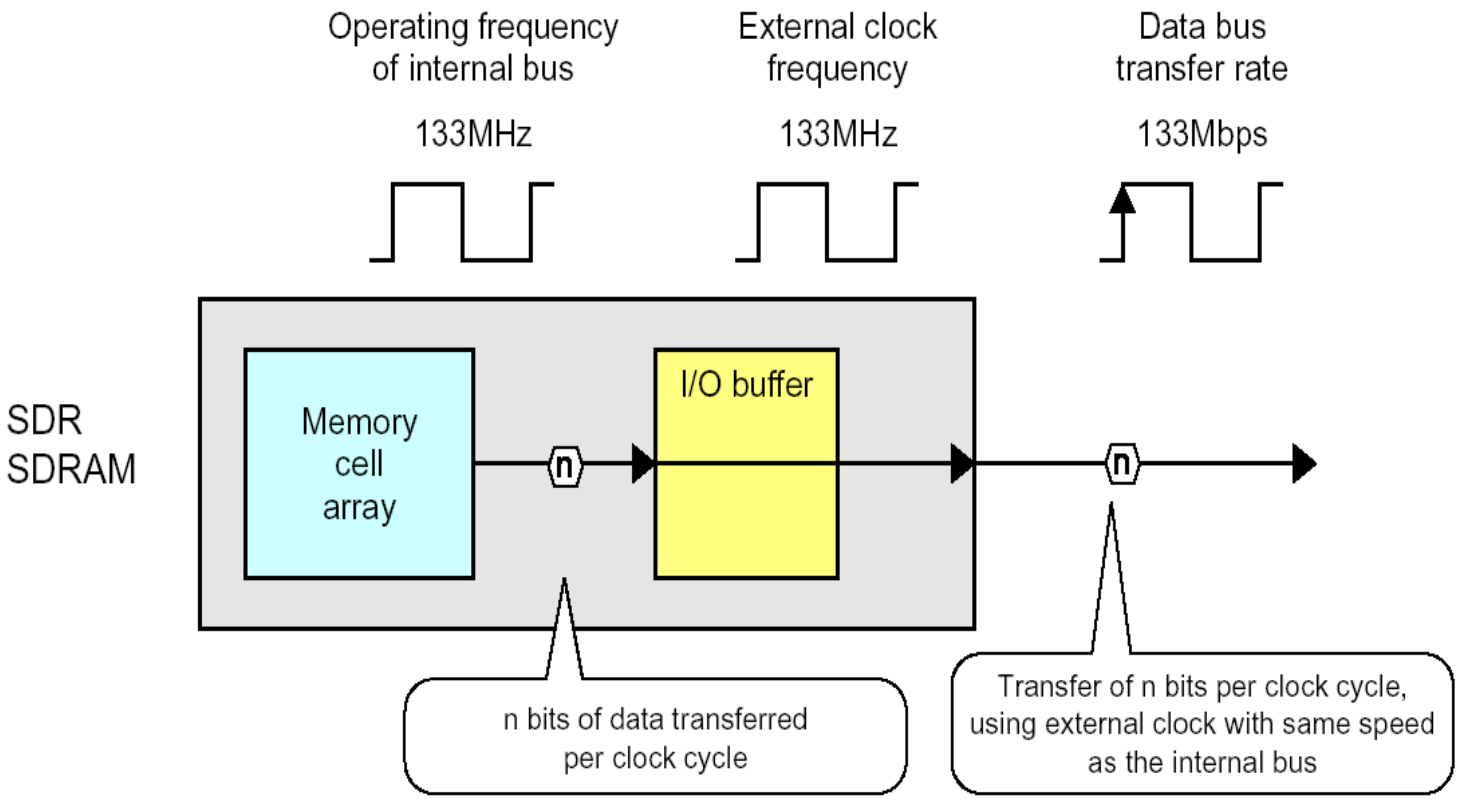
Clock in Synchronous DRAM

- SDRAM Clock: rising edge only
- DDR Clock: both edge
  internal bus size = 2* external
  internal f = 1/2 *ext. f
- DDR2 Clock: both edge
  internal bus size = 4* external
  internal f = 1/4 *ext. f

DDR Clock use

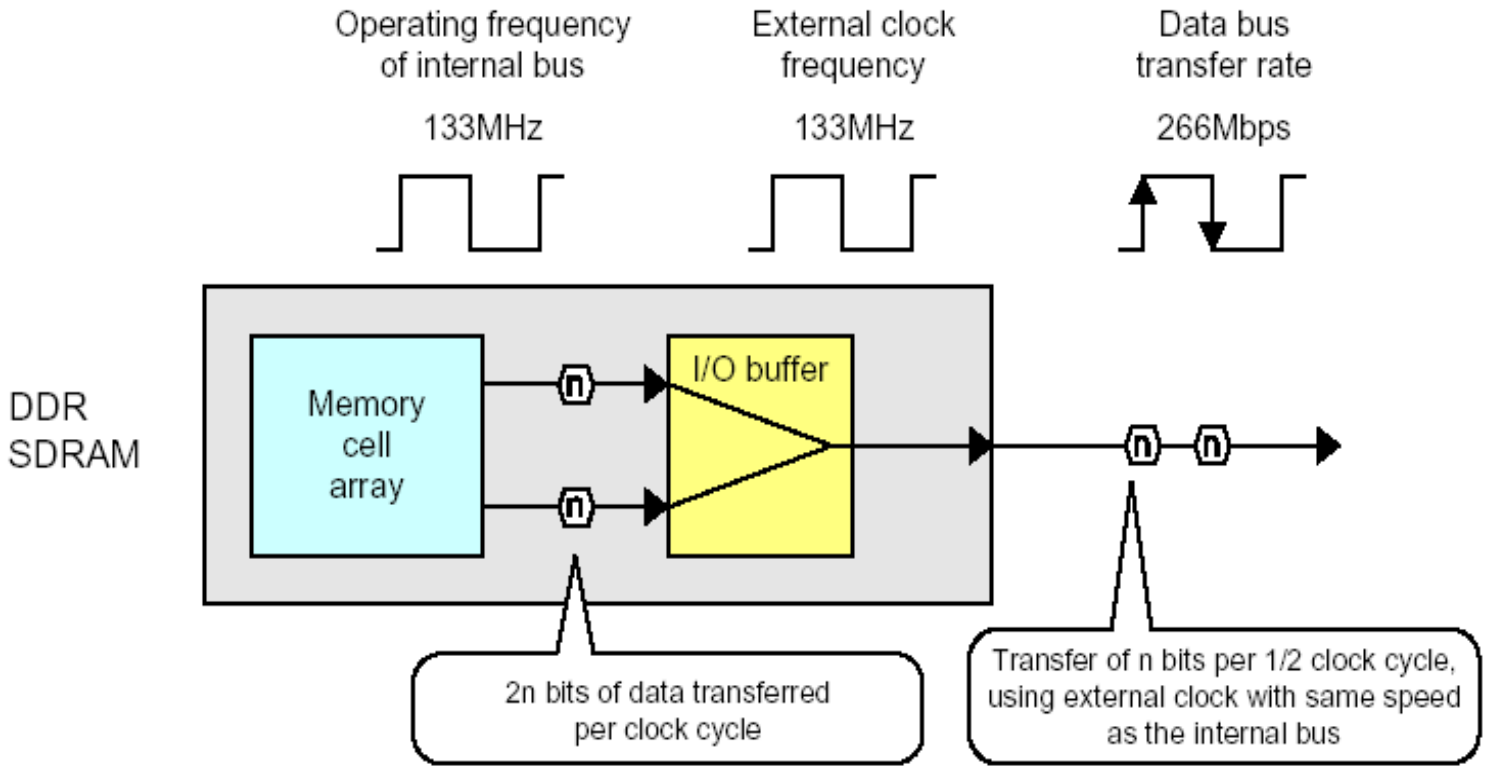
- SDRAM / DDR are synchronous DRAM
- SDRAM are working on rising-edge only
- DDR are working on both edge of the clk for the burst data transfer on the same row of a bank
- They are external clk and internal clk
- Internal bus width can is growing with new generation

Clk SDRAM



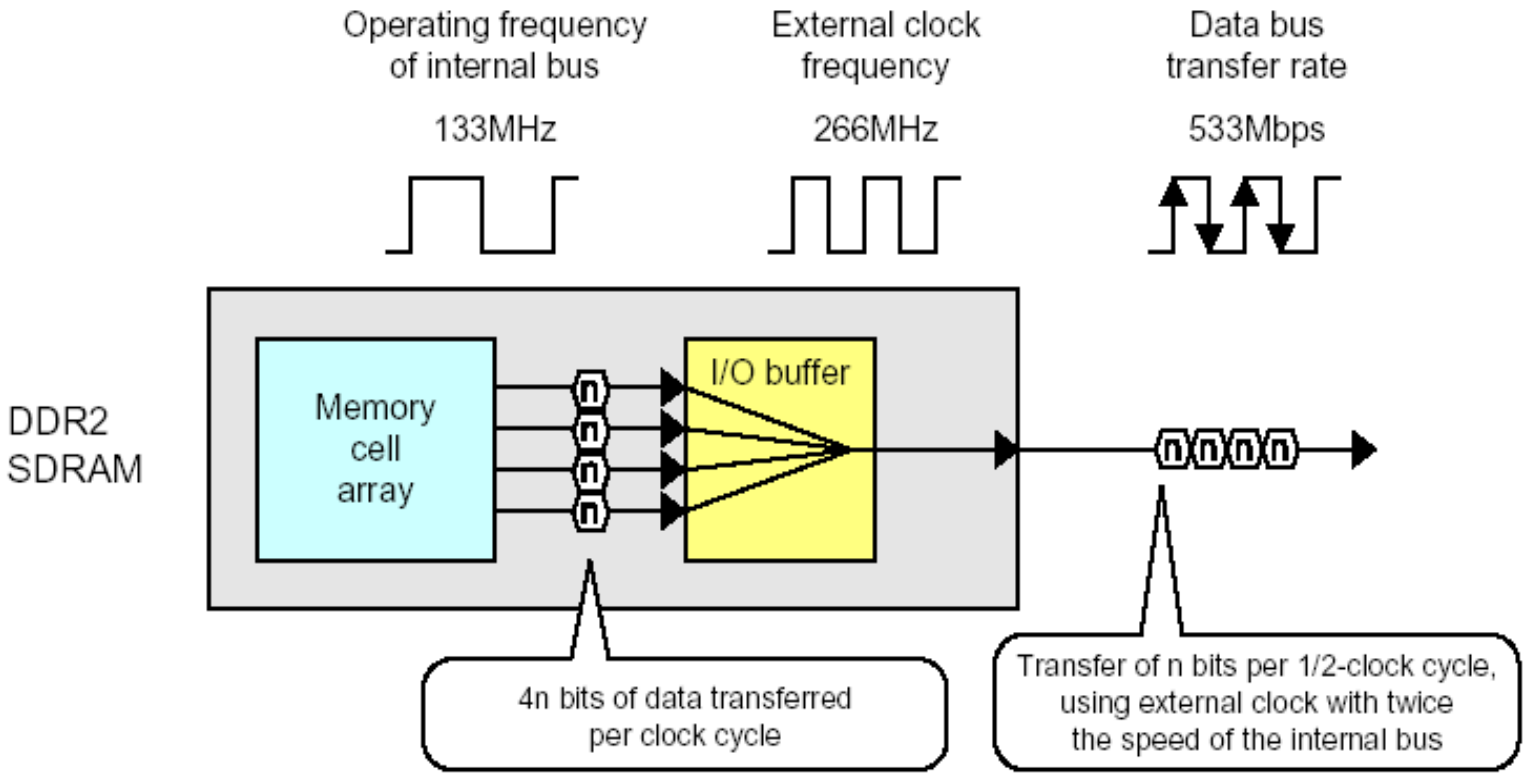
http://www.elpida.com/pdfs/E0437E40.pdf

Clk DDR



http://www.elpida.com/pdfs/E0437E40.pdf

Clk DDR2



http://www.elpida.com/pdfs/E0437E40.pdf

DDR Dual Data Rate

- Synchronization for data transfers : DQs
- Burst transfer on 2 edges of DQs
- Synchronization with DQs :
  - DQs provided by the *memory controller* in write cycle
  - DQs provided by the *memory* in read cycle

  - DQs propagate in the same direction as data
  - DDR : power supply 2.5V
  - DDR-II : power supply 1.8V, ODT (On Die Termination)
  - DDR-III : power supply 1.5V, ODT
  - Data bus termination $V_{tt} = V_{alim}/2$

DDR Dual Data Rate

	DDR SDRAM	DDR2 SDRAM	DDR3 SDRAM
Data Rate	200 / 266 / 333 / 400 Mbps	400 / 533 / 667 / 800 Mbps	800 / 1066 / 1333 / 1600 Mbps
Supply Voltage	2.5V ± 0.2V	1.8V ± 0.1V	1.5V ± 0.075V
Interface	SSTL_2	SSTL_18	SSTL_15
Data Strobe	Single ended	Single ended / Differential	Differential Default
Burst Length	2, 4, 8	4, 8	4 (Burst Chop), 8
Prefetch	2	4	8
Number of Bank	4	4 / 8	8
Reset	No	No	Yes
On Die Termination	No	Yes	Yes (Dynamic ODT)
Driver Calibration	-	Off-Chip Driver Calibration	Self Calibration with ZQ Pin
Package	TSOP II	FBGA	FBGA
RoHS	Support	Support	Support

DDR signaling

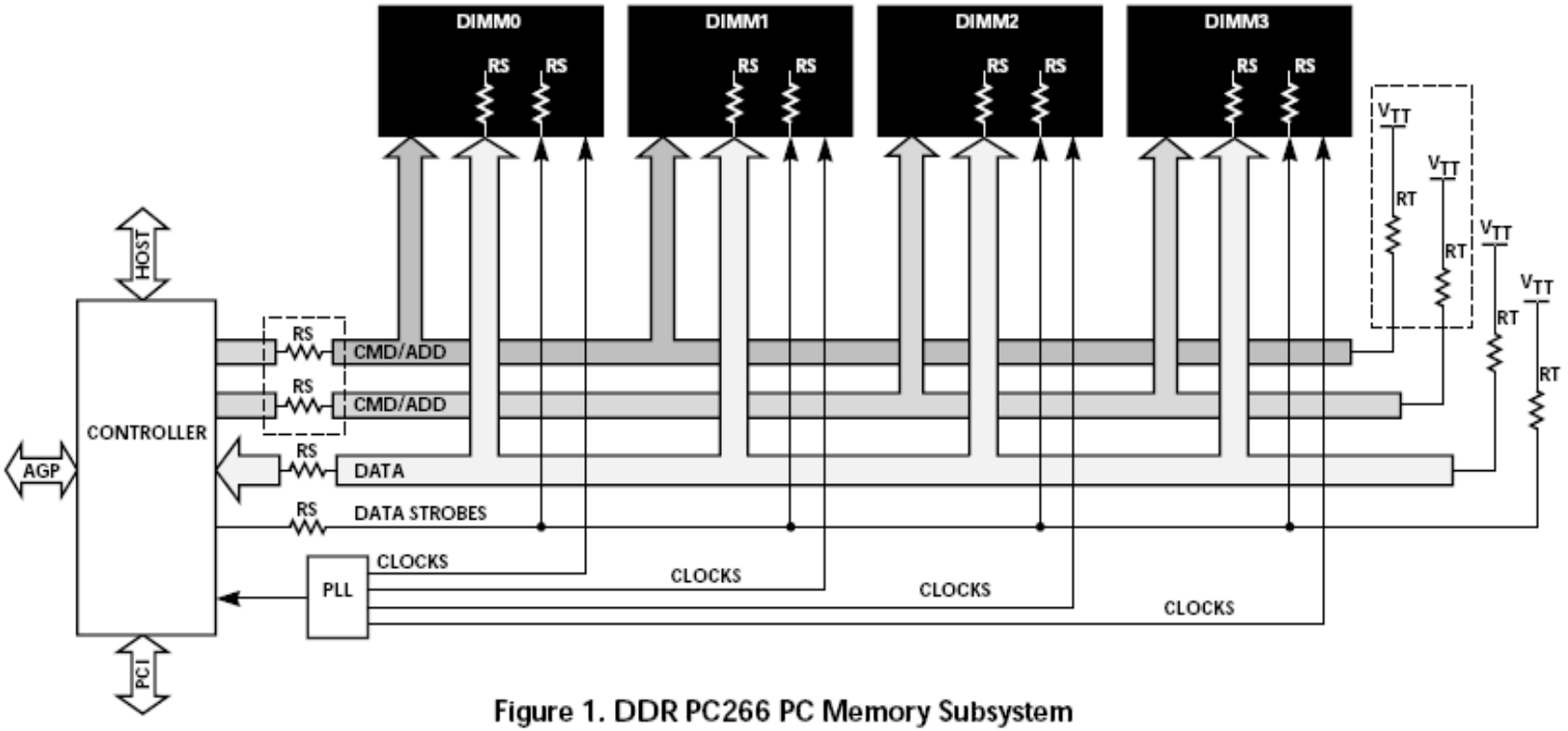
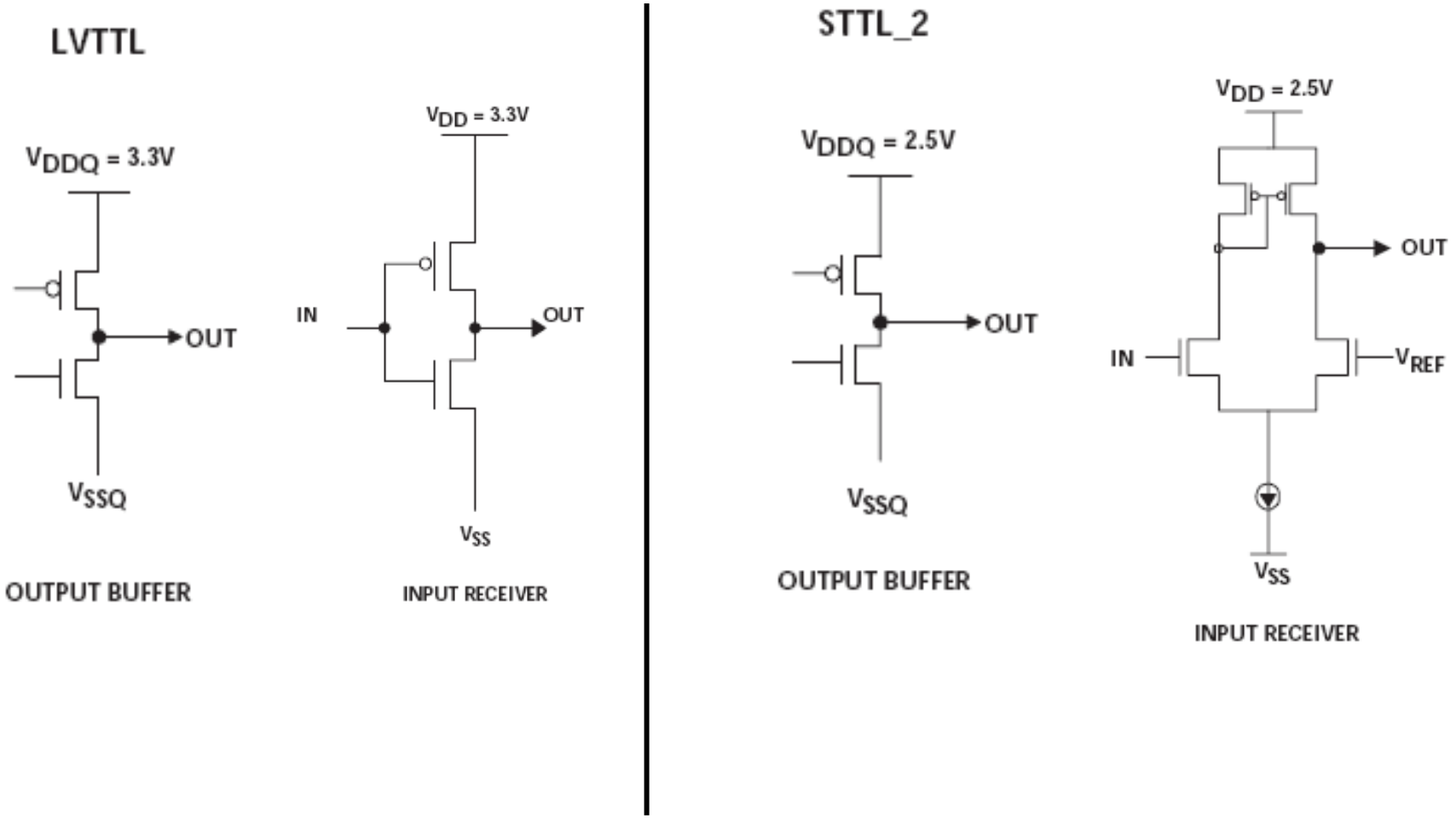


Figure 1. DDR PC266 PC Memory Subsystem

http://www.fairchildsemi.com/ms/MS/MS-6500.pdf

DDR signaling



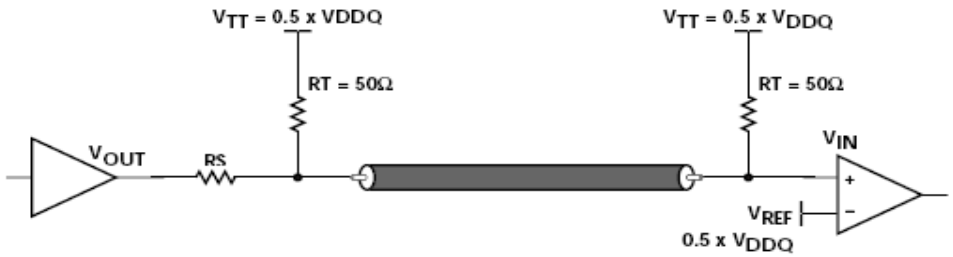
http://www.fairchildsemi.com/ms/MS/MS-6500.pdf

DDR signaling

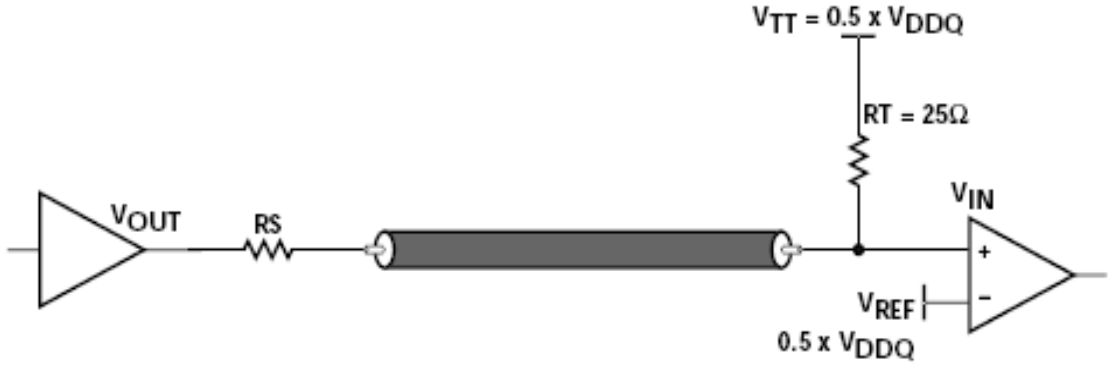
- The SSTL_2 input receiver is typically a **differential pair common source amplifier**. This receiver provides better gain and bandwidth, and the variation in threshold voltage is much tighter, since the threshold voltage offset is determined by identical size and technology transistors in a differential pair configuration.
- The result is that smaller input signal swings can be used reliably.
- Many variations and enhancements to this input receiver topology are in use today.

http://www.fairchildsemi.com/ms/MS/MS-6500.pdf

DDR signaling



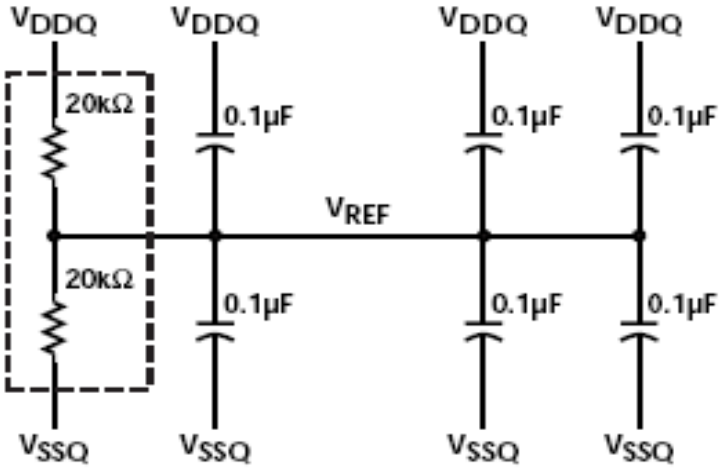
Double terminated output



Single terminated output

http://www.fairchildsemi.com/ms/MS/MS-6500.pdf

DDR signaling



VRef divider and filter

http://www.fairchildsemi.com/ms/MS/MS-6500.pdf

VTT PCB

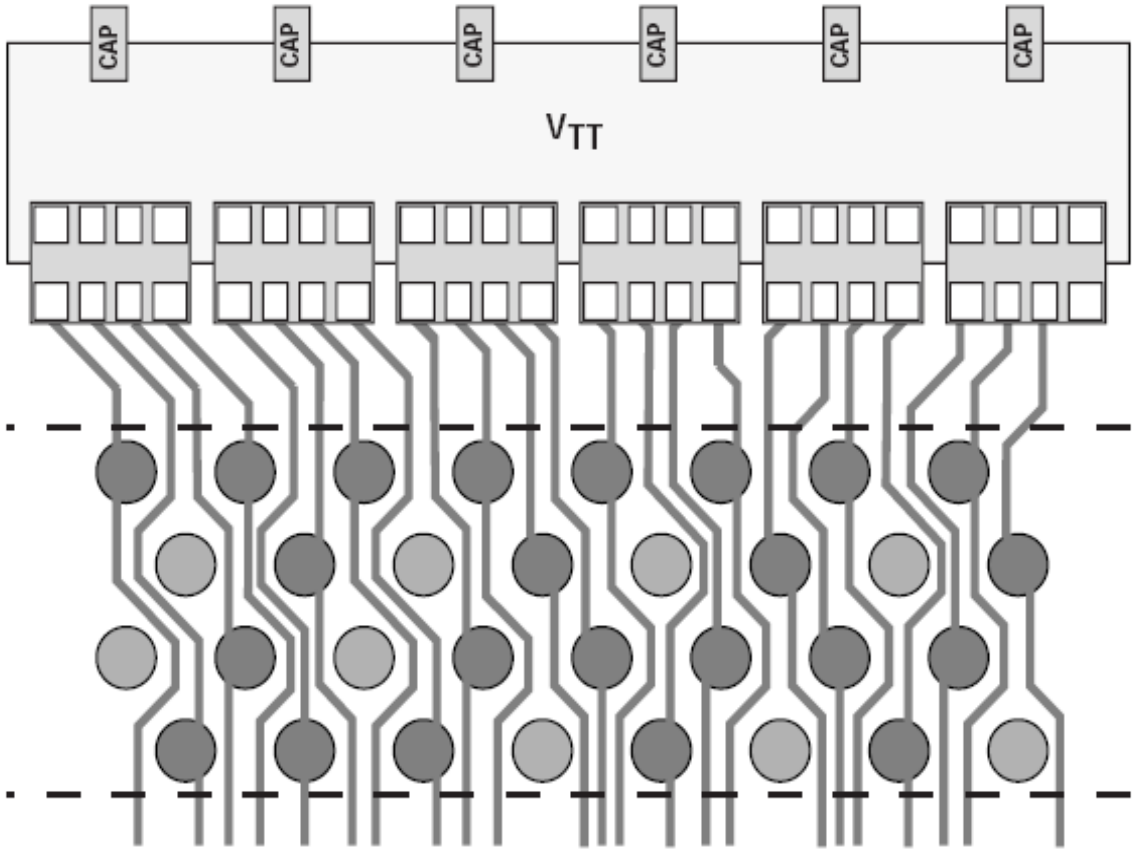
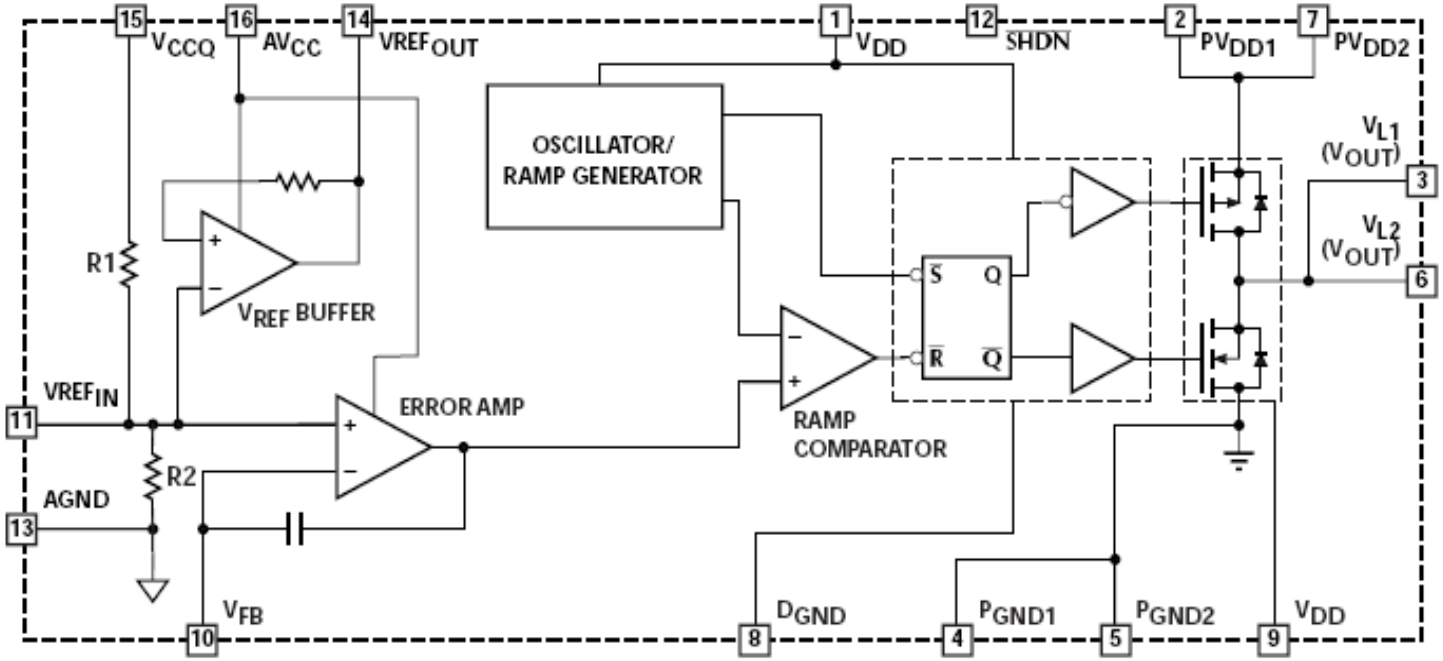


Figure 7. V_{TT} Island PCB Layout

http://www.fairchildsemi.com/ms/MS/MS-6500.pdf

VTT PCB

ML6554 Bus terminator Power

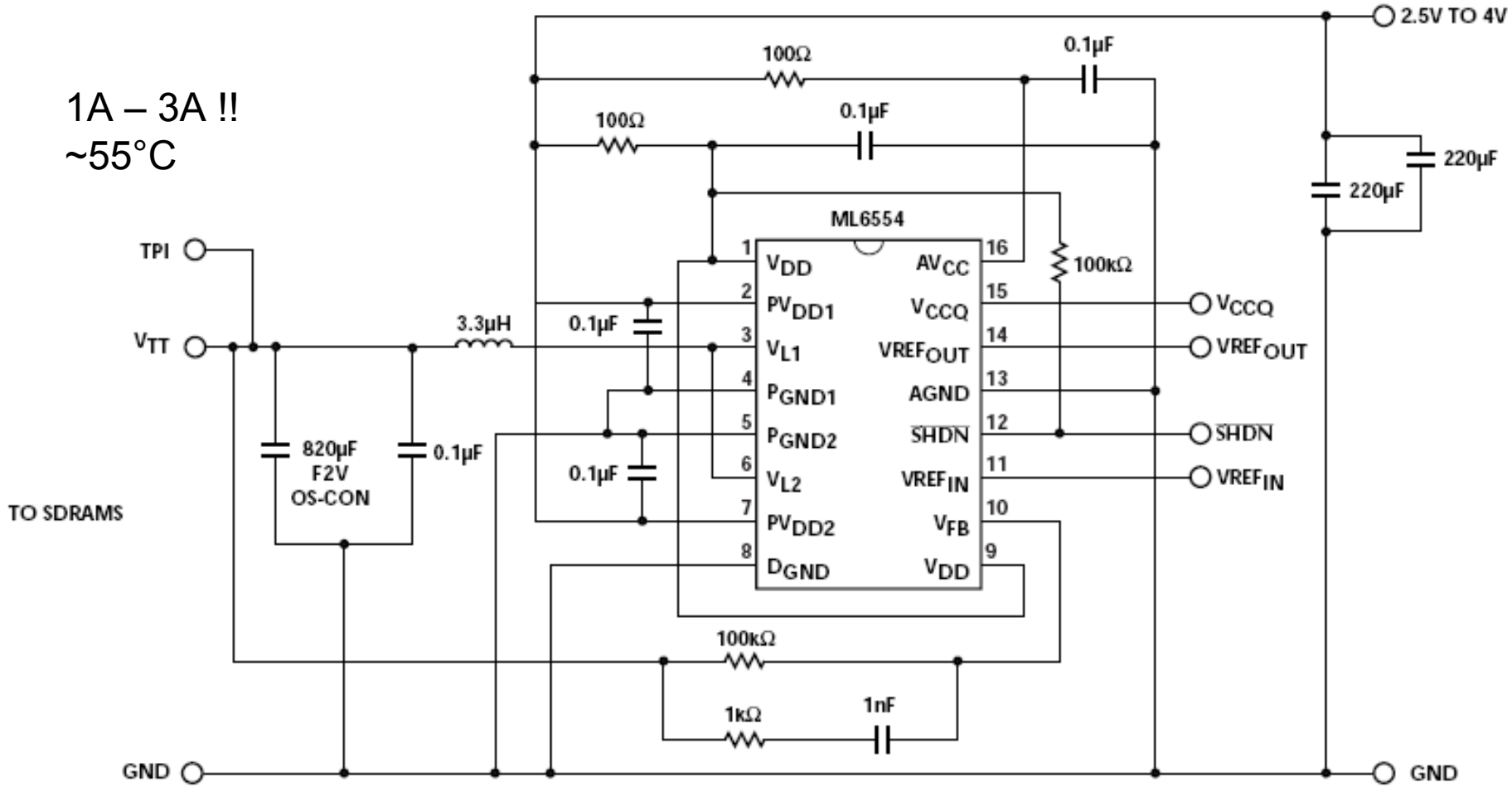


http://www.fairchildsemi.com/ms/MS/MS-6500.pdf

VTT PCB

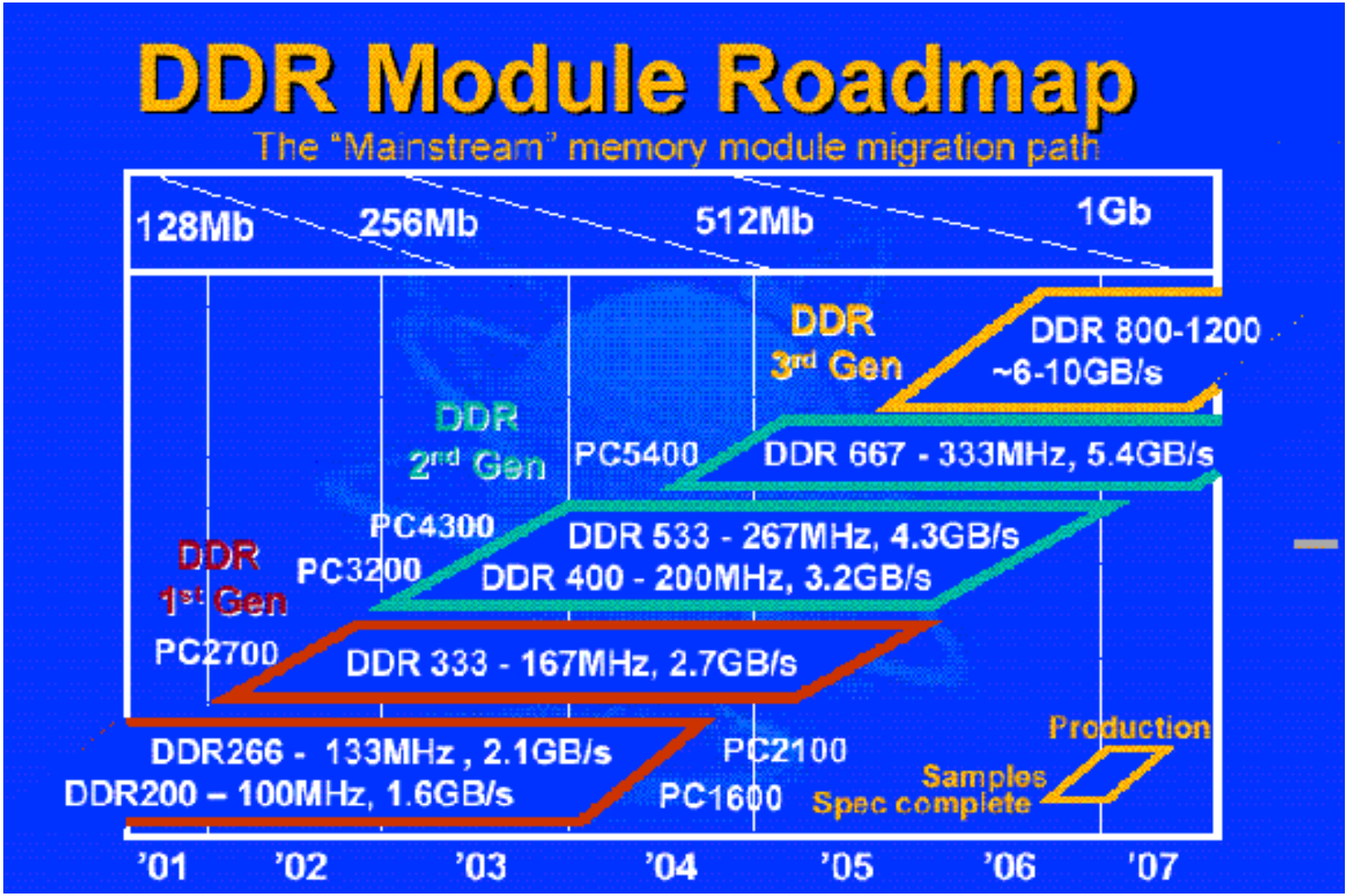
ML6554 Bus terminator Power

1A – 3A !!
~55°C



http://www.fairchildsemi.com/ms/MS/MS-6500.pdf

DDR Dual Data Rate



DDR/RamBus comparison

Memory name	Type name	Clock speed	Voltage	DDR clock speed	Data Bus & Bandwidth
PC100	.	100MHz	3.3v	.	64-bit, 0.8GB/s
PC133	.	133MHz	3.3v	.	64-bit, 1.05B/s
PC1600	DDR200	100MHz	2.5v	200MHz	64-bit, 1.6GB/s
PC2100	DDR266	133MHz	2.5v	266MHz	64-bit, 2.1GB/s
PC2700	DDR333	166MHz	2.5v	333MHz	64-bit, 2.7GB/s
PC3200	DDR400	200MHz	2.5v	400MHz	64-bit, 3.2GB/s
PC4200	DDR533	266MHz	2.5v	533MHz	64-bit, 4.2GB/s
RDRAM PC800	400	400MHz	.	.	16-bit, 1.6GB/s
RDRAM PC1066	533	533MHz	.	.	16-bit, 2.1GB/s
RDRAM PC1200	600	600MHz	.	.	16-bit, 2.4GB/s

SLDRAM (*Synchronous Link DRAM*)

- SLD4M18DR400
- 4Mx18 (75Mbits)
- 400MHz rate
- 800MB/s peak
- 8 internal banks
- Burst 4 or 8
- Protocol paquet oriented
- 2 data clock
- 1 command clock
- Programmable Delay Read/Wite
- 2.5V
- Configuration Register

PIN ASSIGNMENT (Top View)

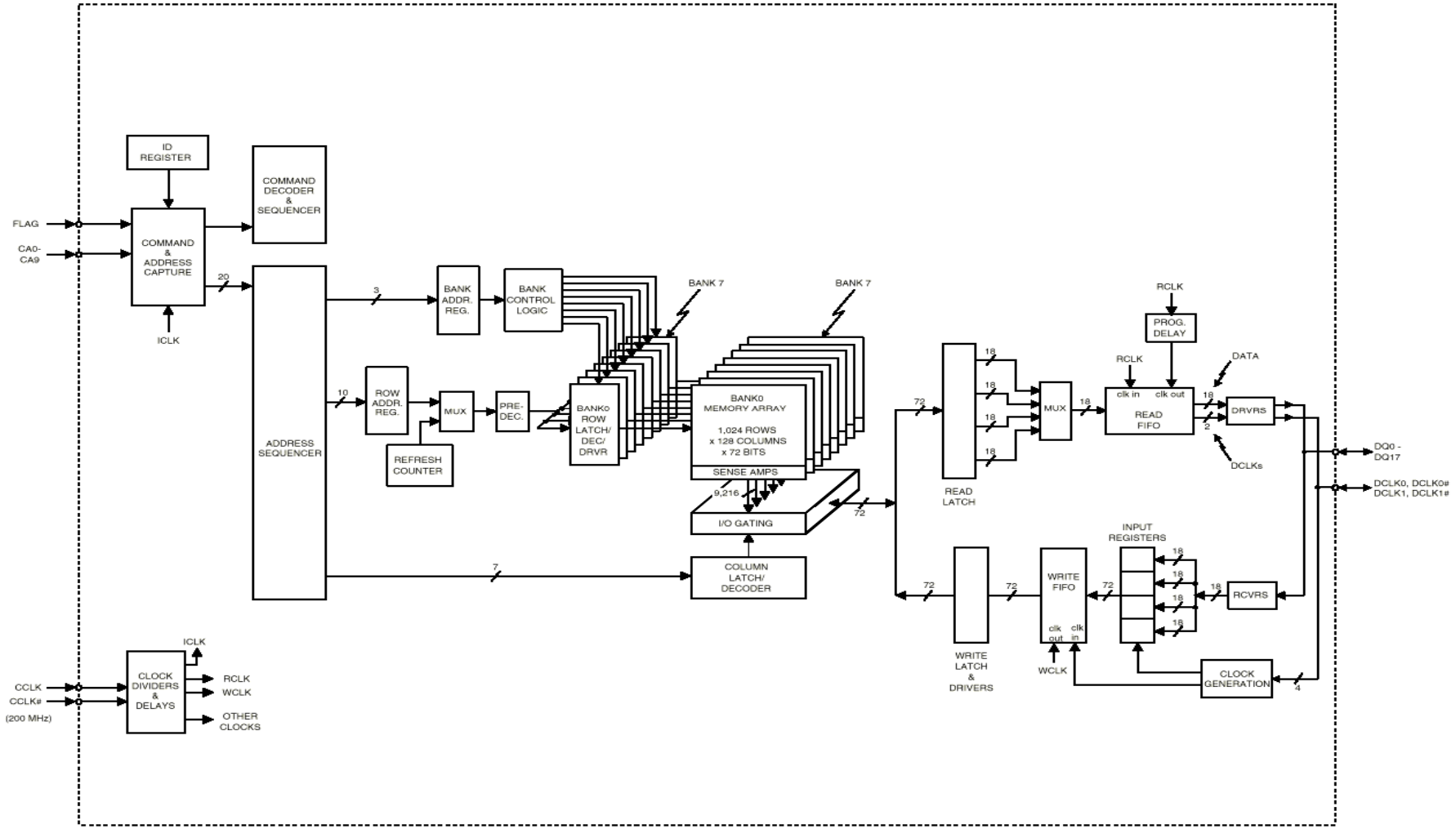
64-Pin HSMP

V_{DD}	1	2	V_{SS}
V_{DD}	3	4	V_{SS}
TEST	5	6	LINKON
RESET#	7	8	LISTEN
V_{DD}	9	10	V_{SS}
V_{DDQ}	11	12	V_{SSQ}
DQ17	13	14	DQ0
DQ1	15	16	DQ2
DQ3	17	18	DQ4
V_{DDQ}	19	20	V_{SSQ}
DQ5	21	22	DQ6
DQ7	23	24	DCLK0#
DCLK0	25	26	DCLK1#
DCLK1	27	28	CCLK#
CCLK	29	30	CA0
CA1	31	32	CA2
V_{DD}	33	34	V_{SS}
CA3	35	36	CA4
CA5	37	38	CA6
CA7	39	40	CA8
CA9	41	42	FLAG
DQ8	43	44	DQ9
DQ10	45	46	V_{SSQ}
V_{DDQ}	47	48	DQ11
DQ12	49	50	DQ13
DQ14	51	52	DQ15
DQ16	53	54	V_{SSQ}
V_{DDQ}	55	56	V_{SS}
V_{DD}	57	58	V_{REF}
SI	59	60	SO
V_{SS}	61	62	V_{DD}
V_{SS}	63	64	V_{DD}

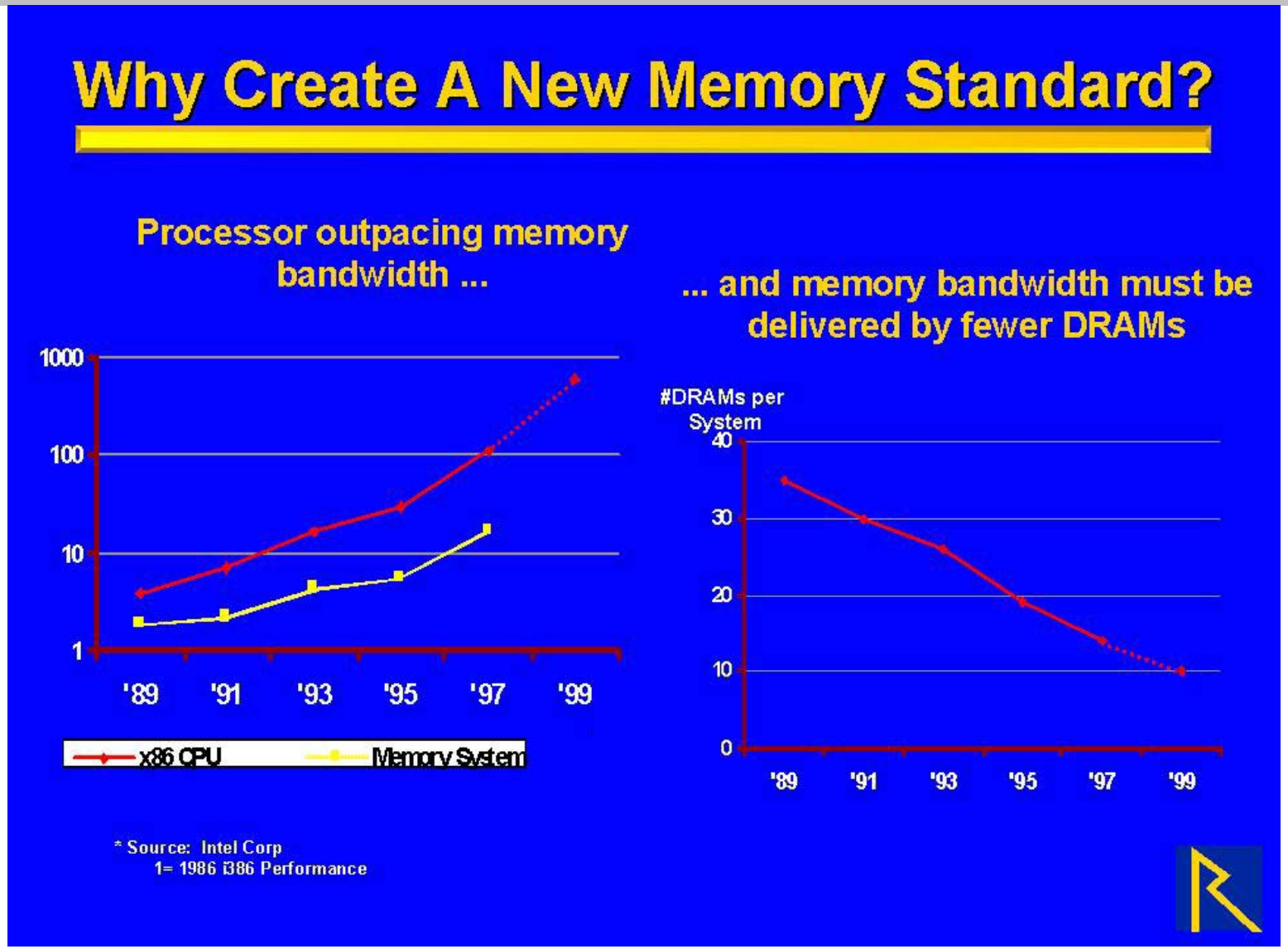
64-Pin VSMP

V_{DD}	1	2	V_{SS}
V_{DD}	3	4	V_{SS}
TEST	5	6	LINKON
RESET#	7	8	LISTEN
V_{DD}	9	10	V_{SS}
V_{DDQ}	11	12	V_{SSQ}
DQ17	13	14	DQ0
DQ1	15	16	DQ2
DQ3	17	18	DQ4
V_{DDQ}	19	20	V_{SSQ}
DQ5	21	22	DQ6
DQ7	23	24	DCLK0#
DCLK0	25	26	DCLK1#
DCLK1	27	28	CCLK#
CCLK	29	30	CA0
CA1	31	32	CA2
V_{DD}	33	34	V_{SS}
CA3	35	36	CA4
CA5	37	38	CA6
CA7	39	40	CA8
CA9	41	42	FLAG
DQ8	43	44	DQ9
DQ10	45	46	V_{SSQ}
V_{DDQ}	47	48	DQ11
DQ12	49	50	DQ13
DQ14	51	52	DQ15
DQ16	53	54	V_{SSQ}
V_{DDQ}	55	56	V_{SS}
V_{DD}	57	58	V_{REF}
SI	59	60	SO
V_{SS}	61	62	V_{DD}
V_{SS}	63	64	V_{DD}

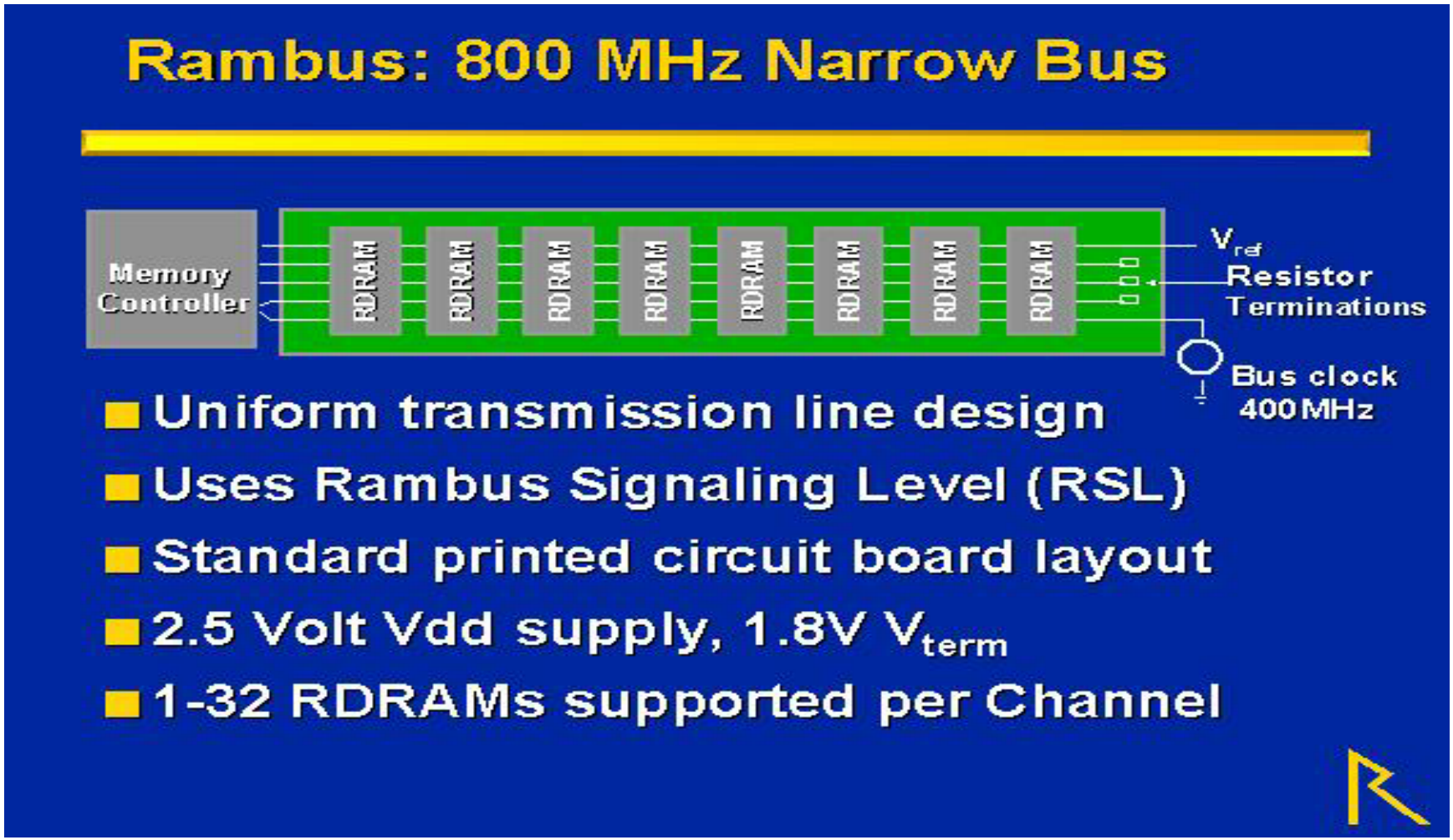
SLDRAM


ID REGISTER
COMMAND DECODER & SEQUENCER
FLAG
CA0-CA9
COMMAND & ADDRESS CAPTURE
20
ICLK
ADDRESS SEQUENCER
3
BANK ADDR. REG.
BANK CONTROL LOGIC
BANK 7
BANK 7
10
ROW ADDR. REG.
MUX
PRE-DEC.
REFRESH COUNTER
BANK0 ROW LATCH/ DEC/ DRVR
BANK0 MEMORY ARRAY
1,024 ROWS
x 128 COLUMNS
x 72 BITS
SENSE AMPS
9,216
I/O GATING
72
7
COLUMN LATCH/ DECODER
READ LATCH
18
MUX
RCLK
PROG. DELAY
RCLK
DATA
clk in
clk out
READ FIFO
DRVRS
DCLKs
DQ0 - DQ17
DCLK0, DCLK0#
DCLK1, DCLK1#
INPUT REGISTERS
WRITE FIFO
clk out
clk in
WCLK
RCVRS
CLOCK GENERATION
WRITE LATCH & DRIVERS
CCLK
CCLK#
(200 MHz)
CLOCK DIVIDERS & DELAYS
ICLK
RCLK
WCLK
OTHER CLOCKS

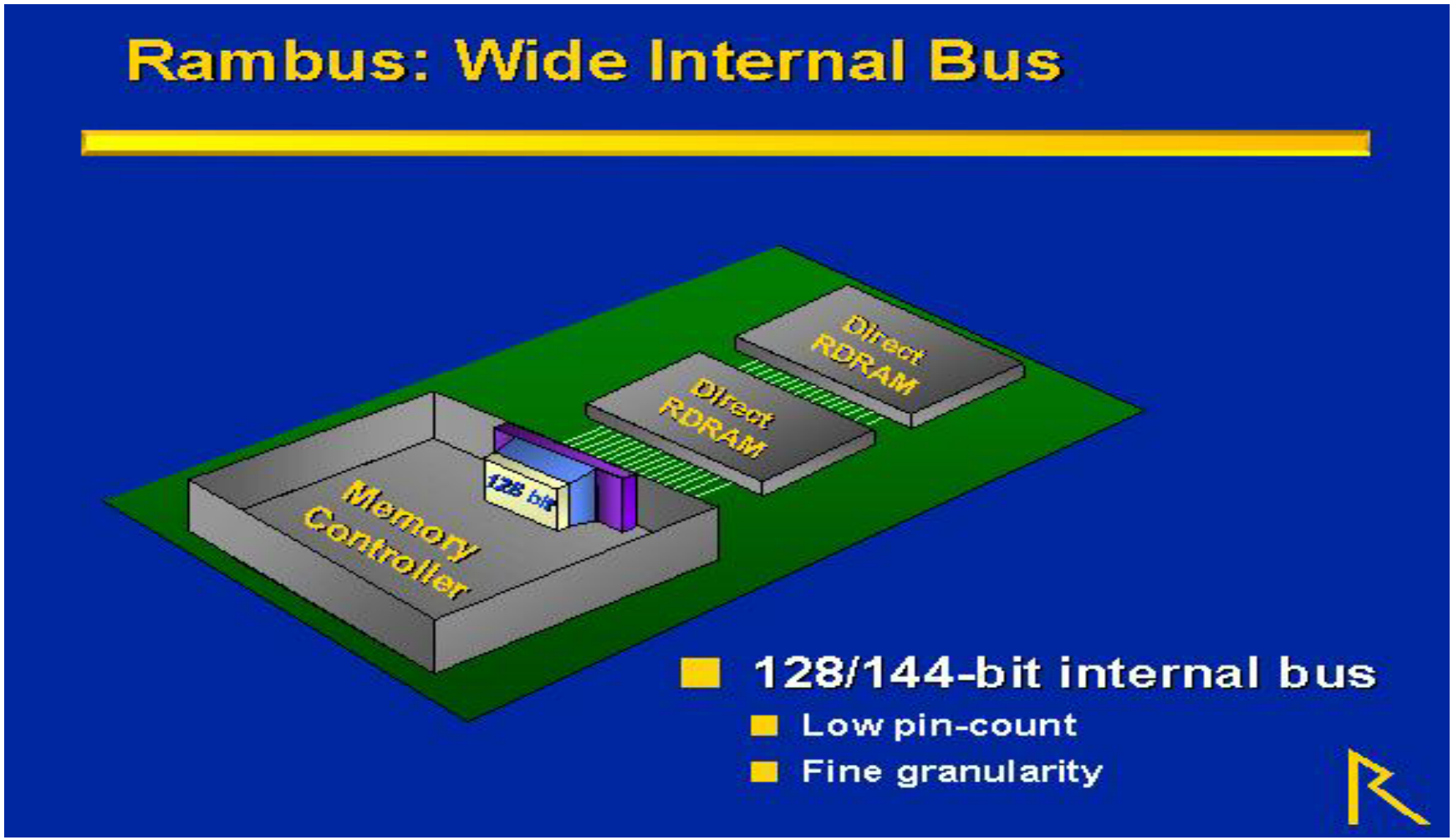
RamBus RDRAM



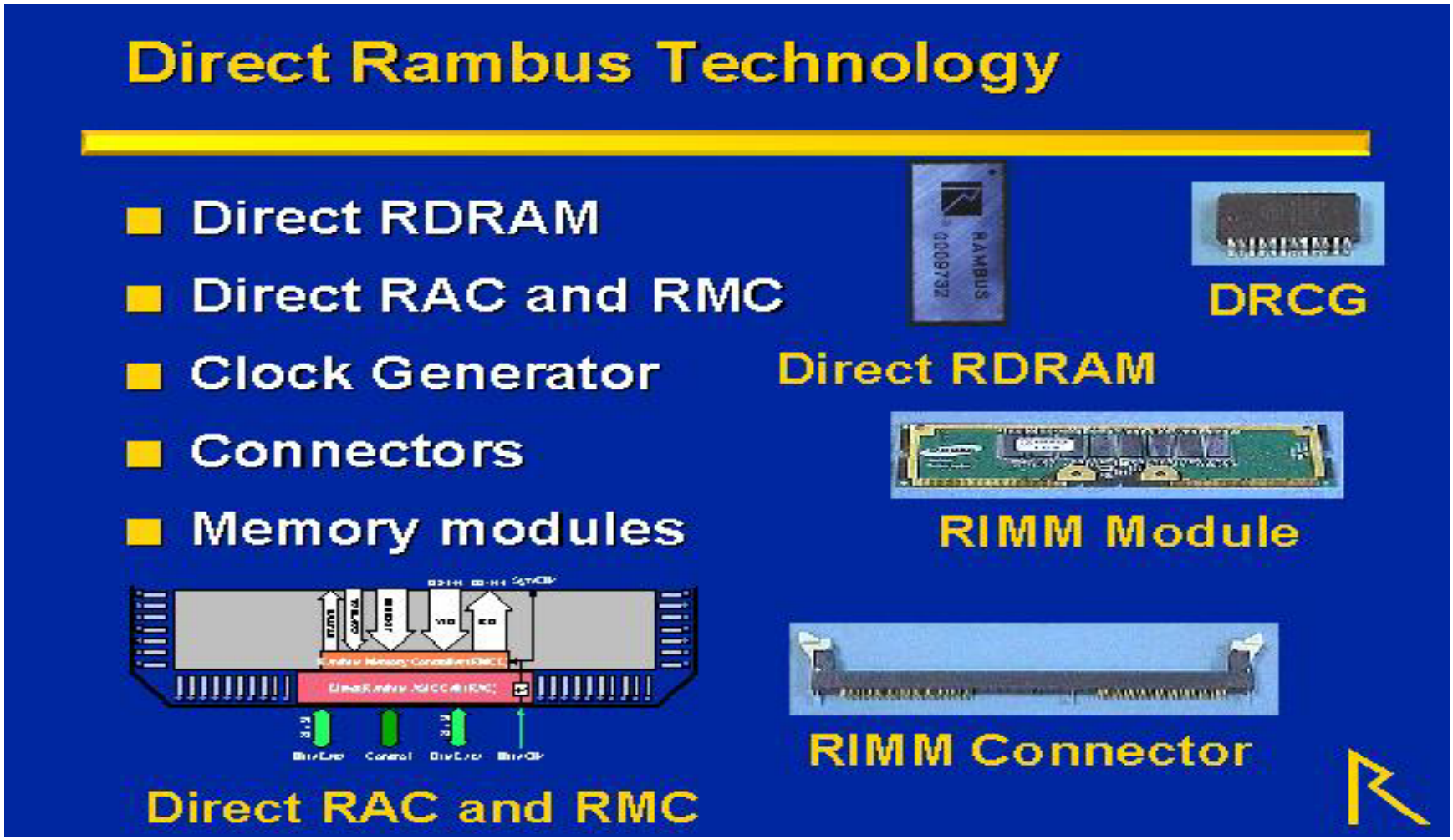
RamBus RDRAM



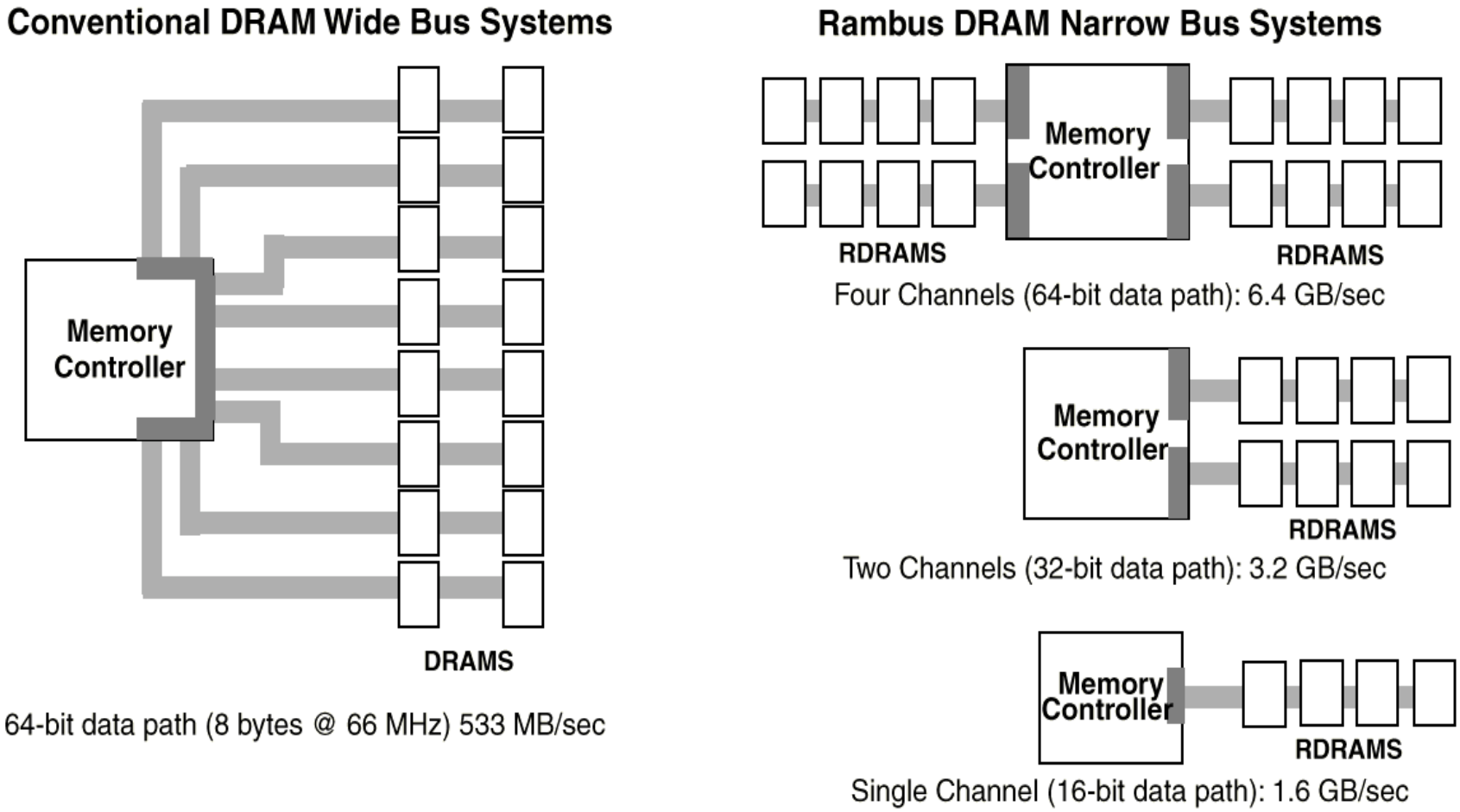
RamBus RDRAM



RamBus RDRAM



RamBus RDRAM

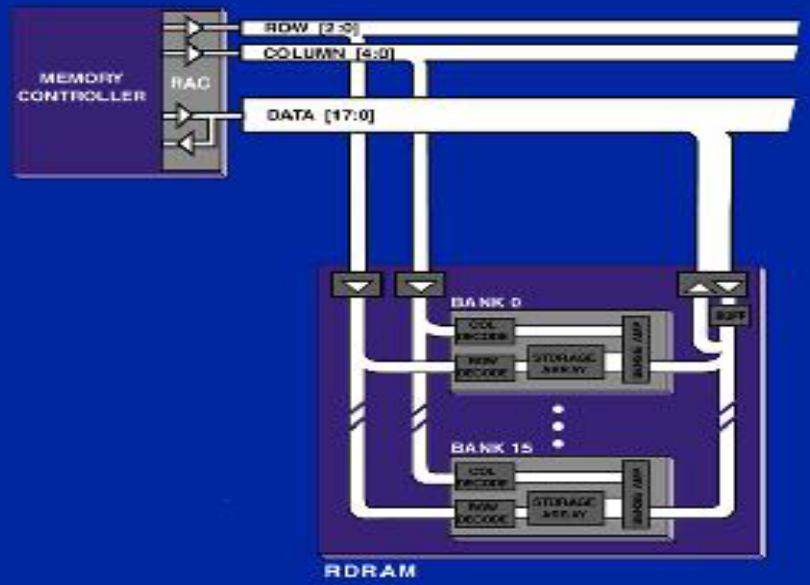


RamBus RDRAM

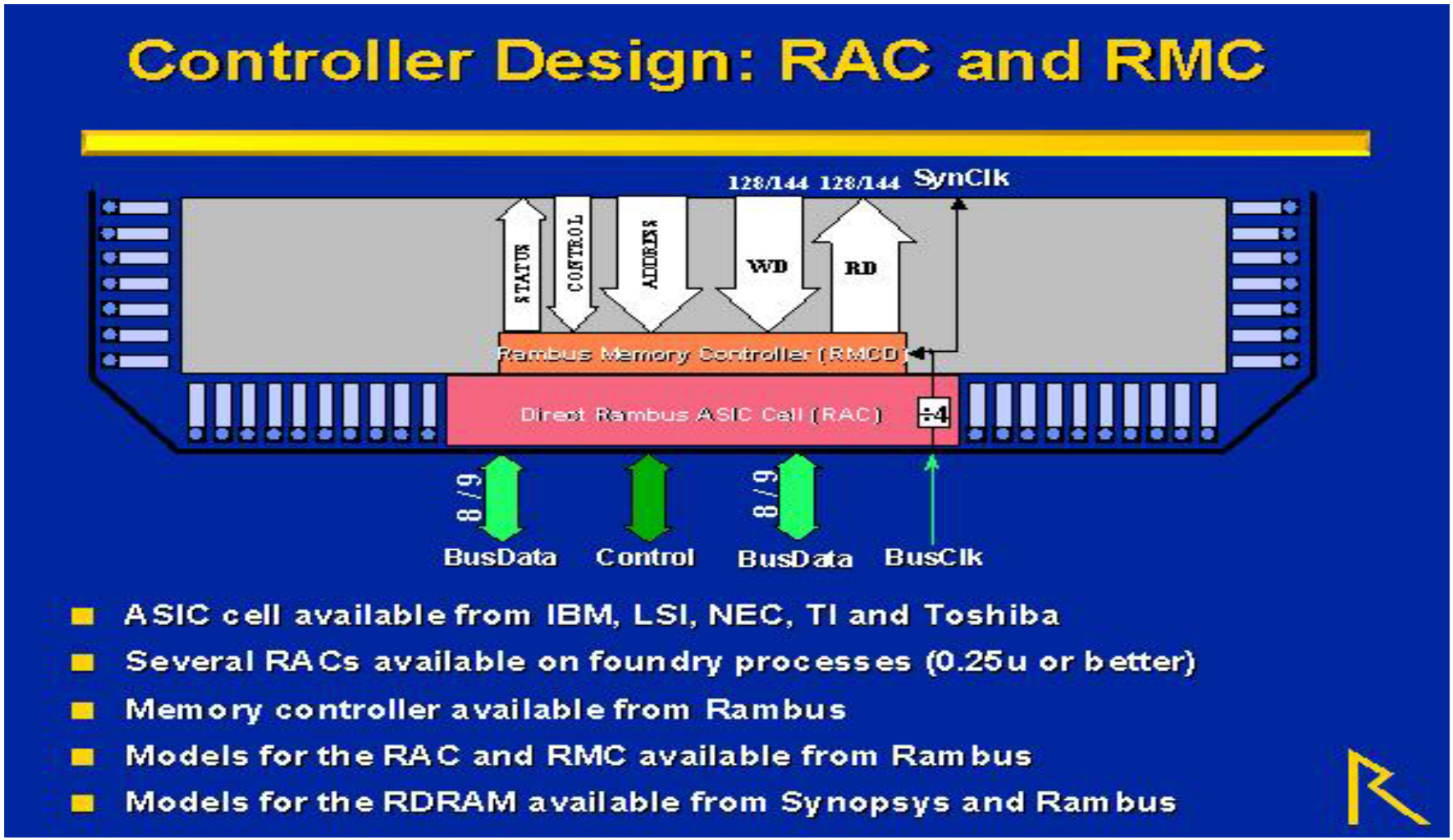
High Channel Efficiency

>95% Channel utilization

- Goal: Maximize number of simultaneous transactions
- Memory system is a pipeline
- Independent resources
  - Row, column, data
  - Lots of banks per DRAM
- Few gaps on data bus



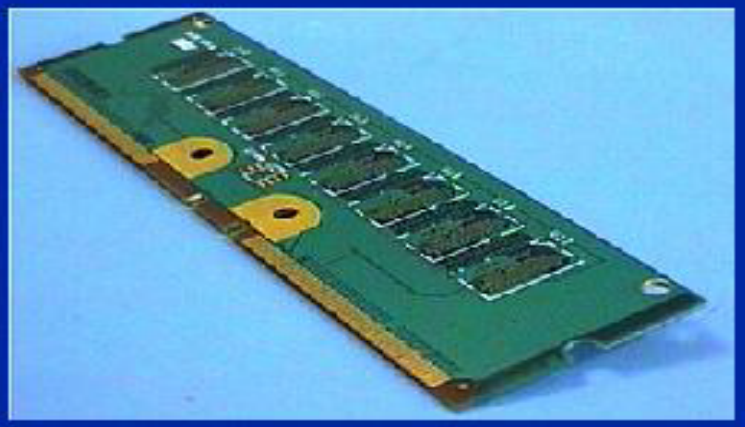
RamBus RDRAM



RamBus RDRAM

Packaging - Industry Standard

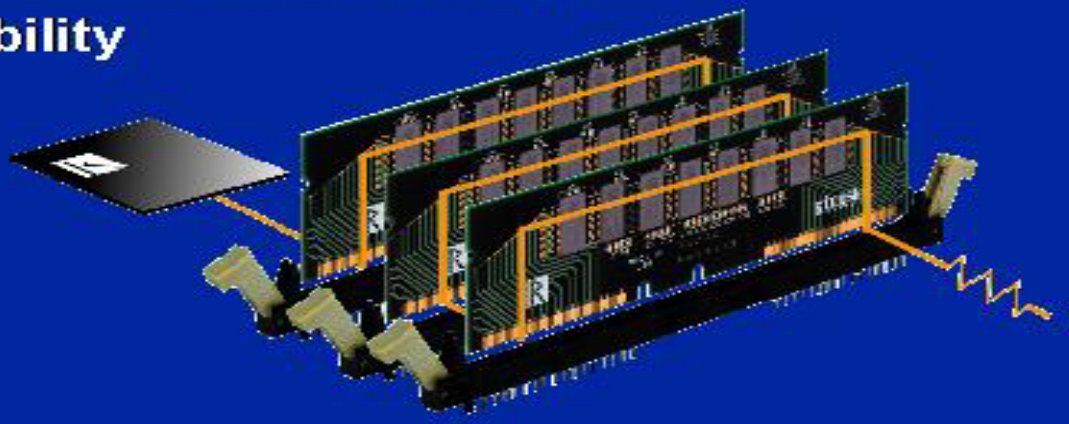
- Rambus RIMM™ modules fit within SDRAM-100 power, thermal envelope
- RDRAM package - chip scale
- DIMM-like module form factor
- DIMM-like connectors



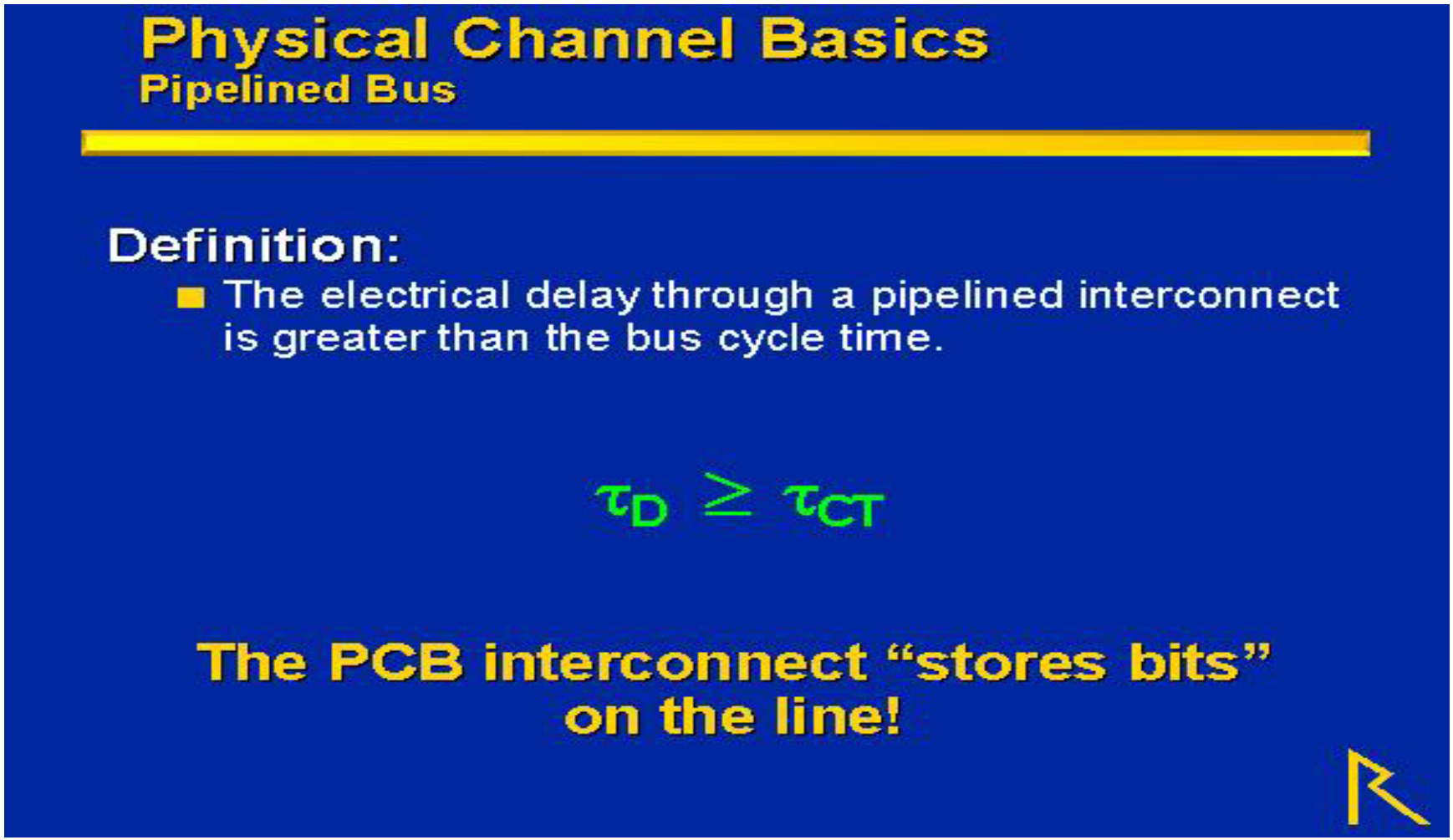
RamBus RDRAM

Direct Rambus Memory

- Highly efficient memory control pipeline
- High bandwidth DRAM core
- Comprehensive infrastructure support
- Broad applicability



RamBus RDRAM



RamBus RDRAM

Channel: Transmission Line

RDRAM capacitance lowers line impedance

- **RESULT: Closely spaced RDRAMs create a "loaded" transmission line impedance**
  - Loaded impedance sets network impedance
    - "Unloaded" line sections and termination must equal loaded impedance.

$$Z0_L = Z0_U = R_{TERM}$$

  - Direct RDRAM Channel impedance is 28 Ohms

RIMM module design guidelines optimize Channel performance