Real Time Embedded Systems

CycloneV & DE1-SoC

René Beuchat
Laboratoire d'Architecture des Processeurs

rene.beuchat@epfl.ch

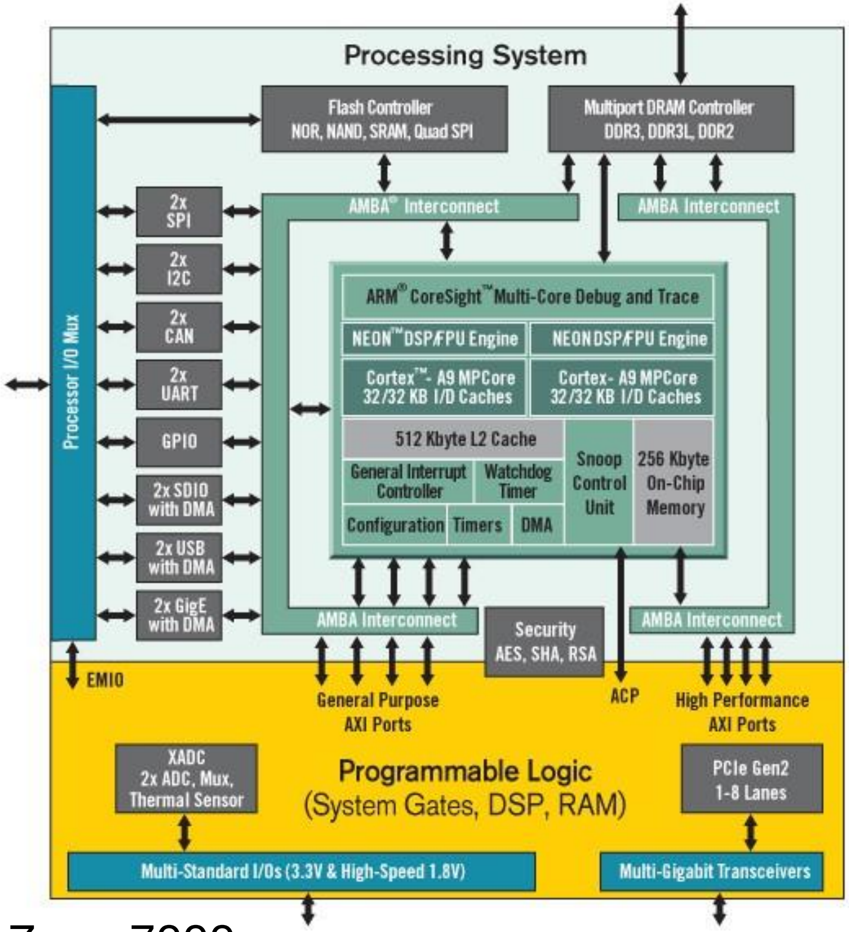
FPGA WITH SOC ARCHITECTURE

2 main actors

- IntelFPGA (Altera (www.altera.com))
  - ➢Cyclone V SOC, Cyclone 10
  - ➢Arria V SOC, Arria 10
  - ➢Stratix 10
- Xilinx (www.xilinx.com)::
  - ➢ Zynq® 7000 family
  - ➢Zynq UltraScale+ MPSoC

2 main actors, Common Features

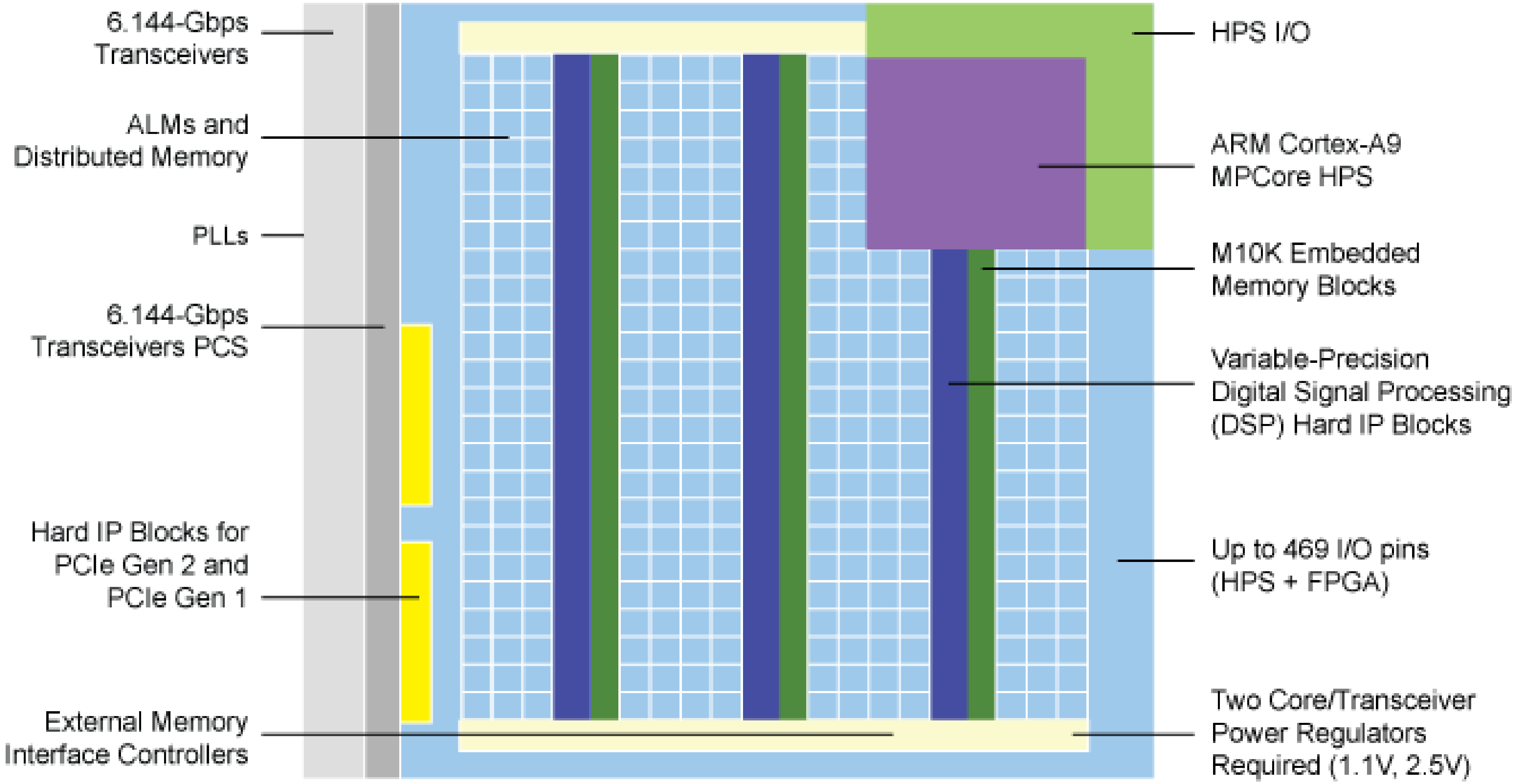
- 2x ARM-Cortex A9 hardcore
  - ➢ 2x NEON DSP/FPU
  - ➢ Many programmable interface in hardcore
  - ➢ Amba interconnect
  - ➢ Large FPGA part
  - ➢ DDR Controller



Ex: Zynq-7000

CYCLONE V-SOC ARCHITECTURE (INTELFPGA)

SOC + FPGA (ex.CycloneV)

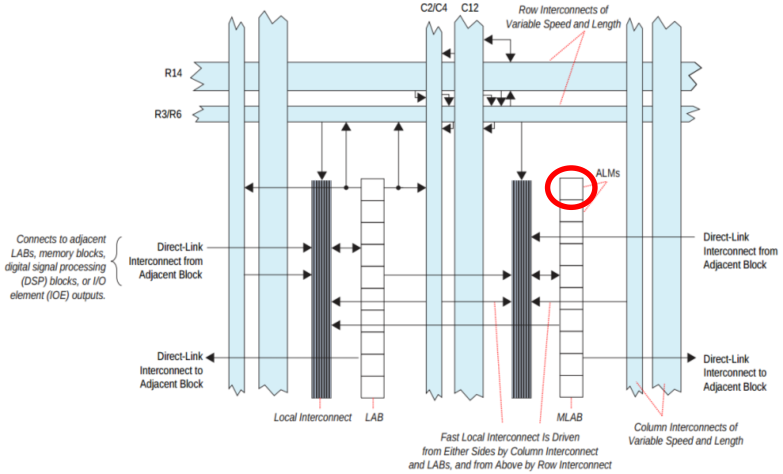

6.144-Gbps Transceivers
ALMs and Distributed Memory
PLLs
6.144-Gbps Transceivers PCS
Hard IP Blocks for PCIe Gen 2 and PCIe Gen 1
External Memory Interface Controllers
HPS I/O
ARM Cortex-A9 MPCore HPS
M10K Embedded Memory Blocks
Variable-Precision Digital Signal Processing (DSP) Hard IP Blocks
Up to 469 I/O pins (HPS + FPGA)
Two Core/Transceiver Power Regulators Required (1.1V, 2.5V)

SOC + FPGA (ex. Cyclone V)

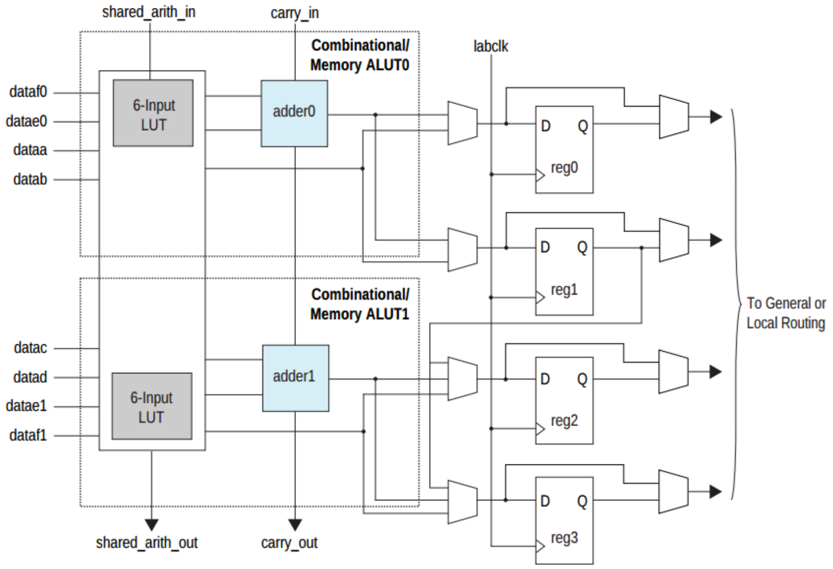
- FPGA part
  - ALM (Adaptative Logic Module)
    - 4 registers
    - Many modes of operations:
      - Normal mode
      - Extended LUT mode
      - Arithmetic mode
      - Shared arithmetic mode
  - Memory (M10k blocks)
  - DSP (Digital Signal Processing) blocks

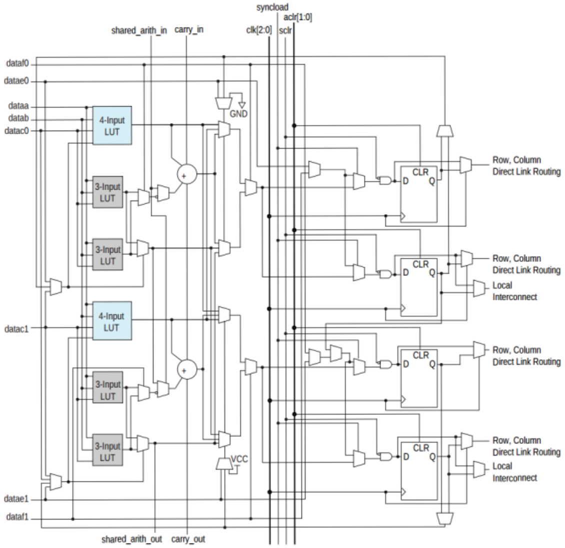
ALM : Adaptative Logic Module

- ALM (Adaptative Logic Module)
- → 32 x 2 Memory Block
- 4 registers



C2/C4
C12
Row Interconnects of Variable Speed and Length
R14
R3/R6
ALMs
Connects to adjacent LABs, memory blocks, digital signal processing (DSP) blocks, or I/O element (IOE) outputs.
Direct-Link Interconnect from Adjacent Block
Direct-Link Interconnect from Adjacent Block
Direct-Link Interconnect to Adjacent Block
Direct-Link Interconnect to Adjacent Block
Local Interconnect
LAB
MLAB
Fast Local Interconnect Is Driven from Either Sides by Column Interconnect and LABs, and from Above by Row Interconnect
Column Interconnects of Variable Speed and Length

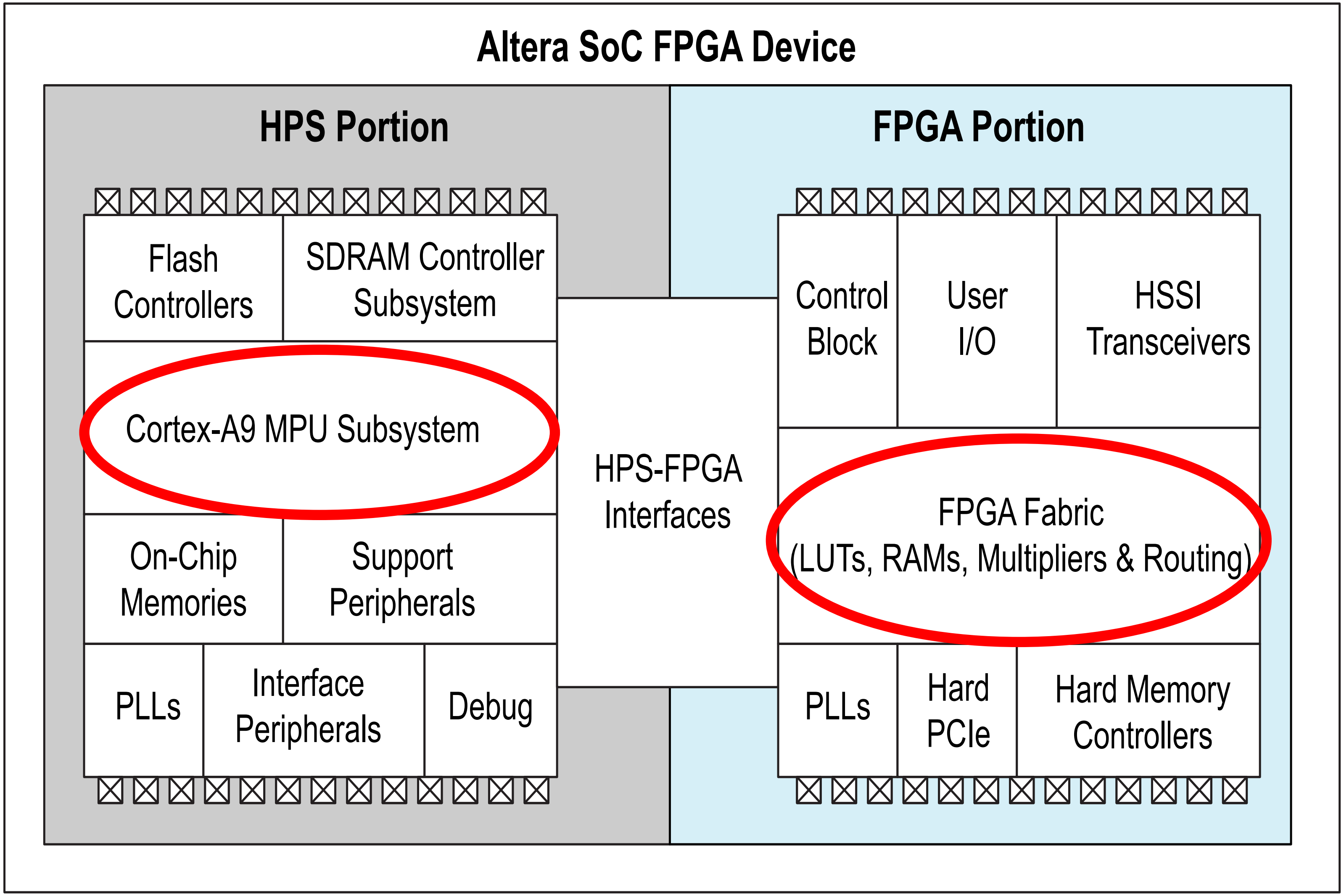




SOC + FPGA (ex. Cyclone V)

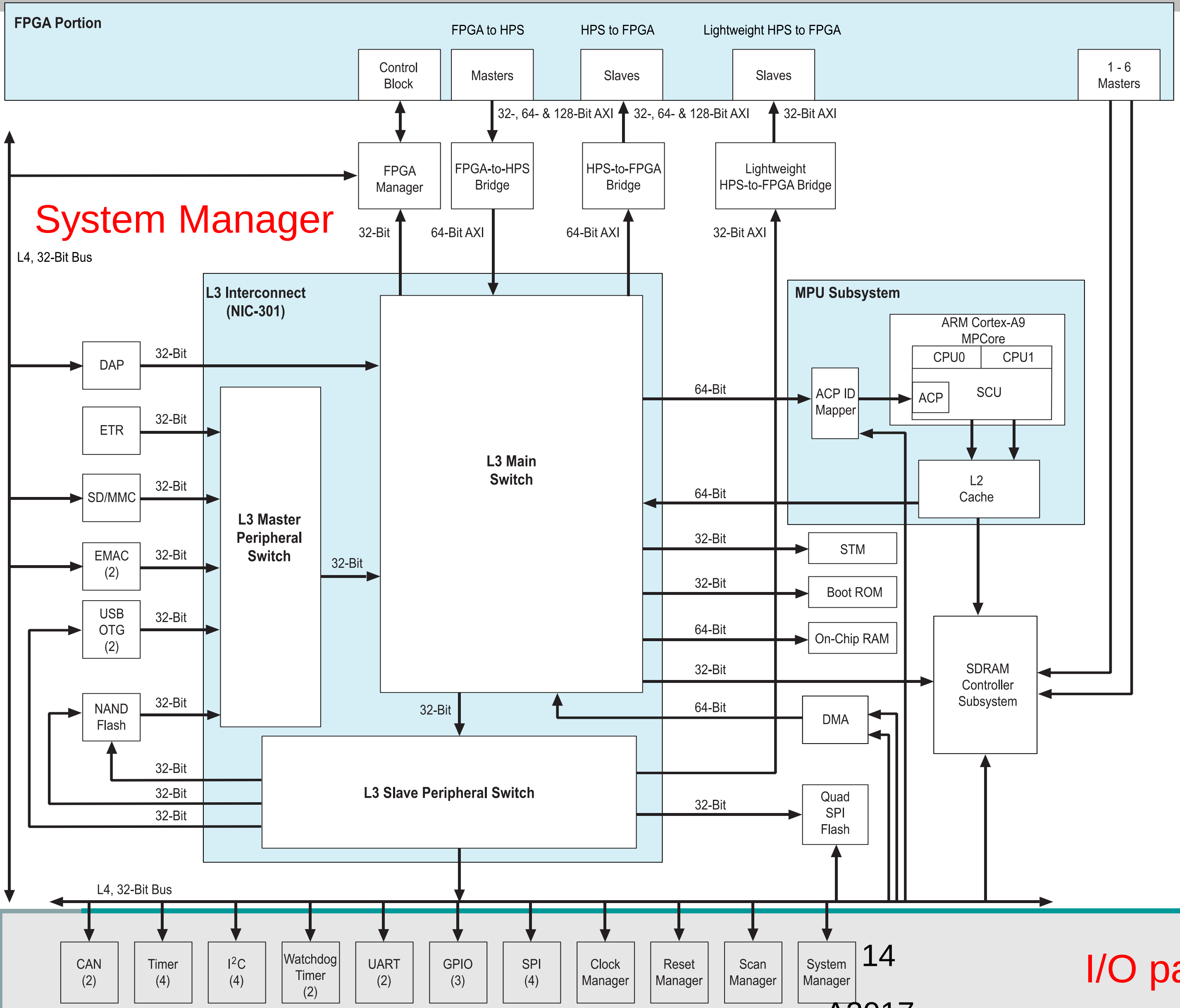
- Hardcore part
  - 2 x ARM Cortex-A9 core
    - + NEON™ SIMD coprocessor
    - +FPU
  - Snoop Control Unit (SCU)
  - Accelerator Coherency Port (ACP)
  - Many programmable interfaces
  - External memory ctrl (DDRx)
  - PCIe (opt.)
  - High speed link (6.144 Gbps) (opt.)
  - HPS I/O

Cyclone V SoC Overview



http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf

Cyclone V HPS (Hard Processor System)

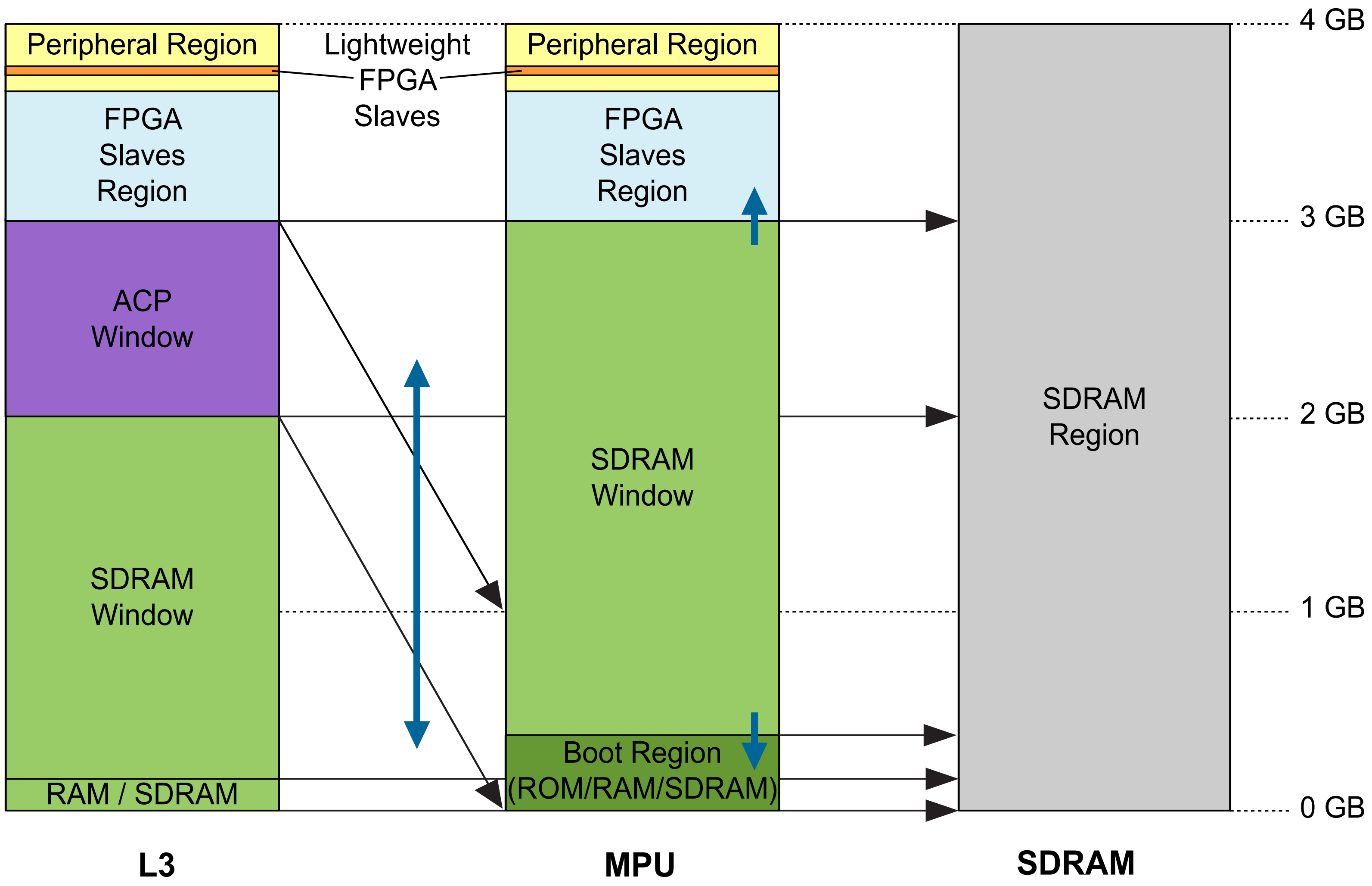


FPGA part

System Manager

I/O part

HPS-FPGA Address Space



HPS L3/MPU Address Space

Region Name	Description	Base Address	Size
FPGA slaves	FPGA slaves connected to the HPS-to-FPGA bridge	0xC000 0000	960 MB
HPS peripherals	Slaves directly connected to the HPS	0xFC00 0000	64 MB
Lightweight FPGA slaves	FPGA slaves connected to the lightweight HPS-to-FPGA bridge	0xFF20 0000	2 MB

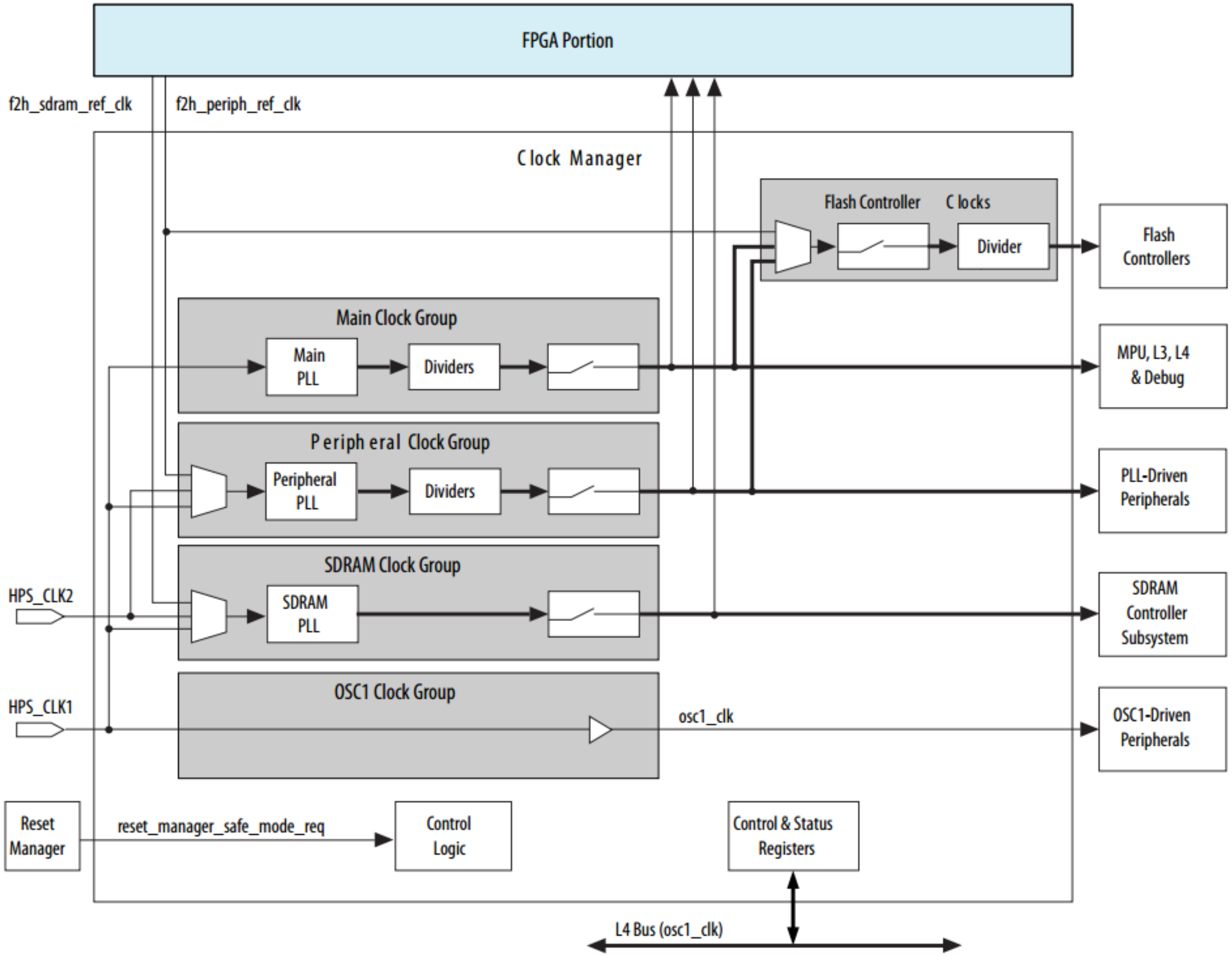
HPS Peripheral Region Address Map

Slave Identifier	Slave Title	Base Address	Size
STM	STM	0xFC00 0000	48 MB
DAP	DAP	0xFF00 0000	2 MB
LWFPGASLAVES	FPGA slaves accessed with lightweight HPS-to-FPGA bridge	0xFF20 0000	2 MB
LWHPS2FPGAREGS	Lightweight HPS-to-FPGA bridge GPV	0xFF40 0000	1 MB
HPS2FPGAREGS	HPS-to-FPGA bridge GPV	0xFF50 0000	1 MB
FPGA2HPSREGS	FPGA-to-HPS bridge GPV	0xFF60 0000	1 MB
EMAC0	EMAC0	0xFF70 0000	8 KB
EMAC1	EMAC1	0xFF70 2000	8 KB
SDMMC	SD/MMC	0xFF70 4000	4 KB
QSPIREGS	Quad SPI flash controller registers	0xFF70 5000	4 KB
FPGAMGRREGS	FPGA manager registers	0xFF70 6000	4 KB
ACPIDMAP	ACP ID mapper registers	0xFF70 7000	4 KB
GPIO0	GPIO0	0xFF70 8000	4 KB
GPIO1	GPIO1	0xFF70 9000	4 KB
GPIO2	GPIO2	0xFF70 A000	4 KB
L3REGS	L3 interconnect GPV	0xFF80 0000	1 MB
NANDDATA	NAND controller data	0xFF90 0000	1 MB
QSPIDATA	Quad SPI flash data	0xFFA0 0000	1 MB
USB0	USB0 OTG controller registers	0xFFB0 0000	256 KB
USB1	USB1 OTG controller registers	0xFFB4 0000	256 KB
NANDREGS	NAND controller registers	0xFFB8 0000	64 KB
FPGAMGRDATA	FPGA manager configuration data	0xFFB9 0000	4 KB

HPS Peripheral Region Address Map

Slave Identifier	Slave Title	Base Address	Size
CAN0	CAN0 controller registers	0xFFC0 0000	4 KB
CAN1	CAN1 controller registers	0xFFC0 1000	4 KB
UART0	UART0	0xFFC0 2000	4 KB
UART1	UART1	0xFFC0 3000	4 KB
I2C0	I2C0	0xFFC0 4000	4 KB
I2C1	I2C1	0xFFC0 5000	4 KB
I2C2	I2C2	0xFFC0 6000	4 KB
I2C3	I2C3	0xFFC0 7000	4 KB
SPTIMER0	SP Timer0	0xFFC0 8000	4 KB
SPTIMER1	SP Timer1	0xFFC0 9000	4 KB
SDRREGS	SDRAM controller subsystem registers	0xFFC2 0000	128 KB
OSC1TIMER0	OSC1 Timer0	0xFFD0 0000	4 KB
OSC1TIMER1	OSC1 Timer1	0xFFD0 1000	4 KB
L4WD0	Watchdog0	0xFFD0 2000	4 KB
L4WD1	Watchdog1	0xFFD0 3000	4 KB
CLKMGR	Clock manager	0xFFD0 4000	4 KB
RSTMGR	Reset manager	0xFFD0 5000	4 KB
SYSMGR	System manager	0xFFD0 8000	16 KB
DMANONSECURE	DMA nonsecure registers	0xFFE0 0000	4 KB
DMASECURE	DMA secure registers	0xFFE0 1000	4 KB
SPIS0	SPI slave0	0xFFE0 2000	4 KB
SPIS1	SPI slave1	0xFFE0 3000	4 KB
SPIM0	SPI master0	0xFFF0 0000	4 KB
SPIM1	SPI master1	0xFFF0 1000	4 KB
SCANMGR	Scan manager registers	0xFFF0 2000	4 KB
ROM	Boot ROM	0xFFFD 0000	64 KB
MPUSCU	MPU SCU registers	0xFFFE C000	8 KB
MPUL2	MPU L2 cache controller registers	0xFFFE F000	4 KB
OCRAM	On-chip RAM	0xFFFF 0000	64 KB

Clock manager



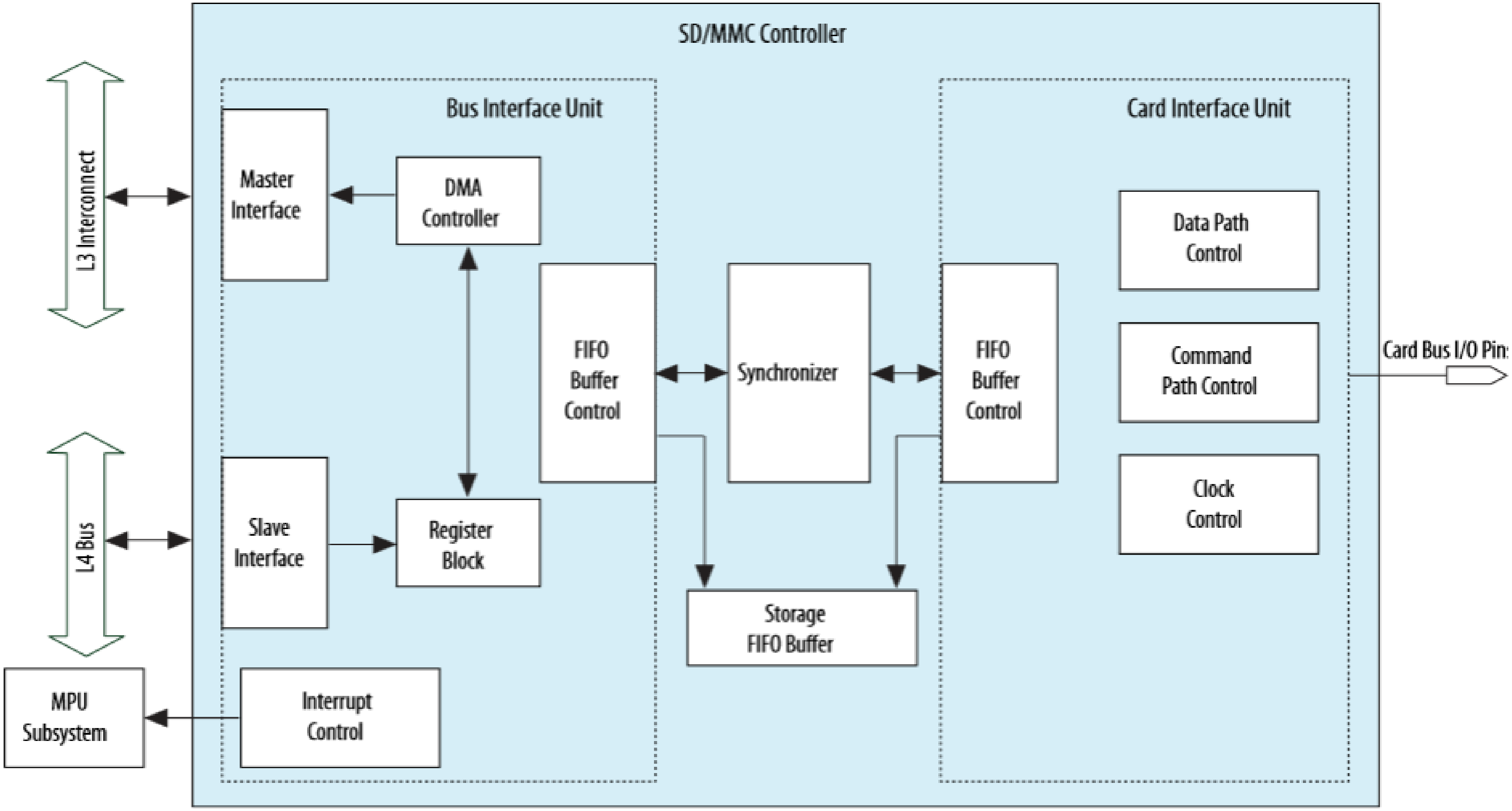
Abbreviation

STM	System Trace Module
DMA	Direct Memory Access
DAP	Debug Access Port
ETR	Embedded Trace Router
SD/	Supporte: SDSC(SD), SDHC, SDXC, eSD, SDIO, eSDIO
MMC	MMC, RSMMC, MMCPlus, MMCMobile, eMMC
EMAC	Ethernet Media Access Controller

Abbreviation

ACP	Accelerator Coherency Port
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver-Transmitter
SPI	Synchronous Peripheral Interface
CAN	Controller Area Network
I2C	Inter-Integrated Circuit

Ex. Programmable Interface SD/MMC Unit

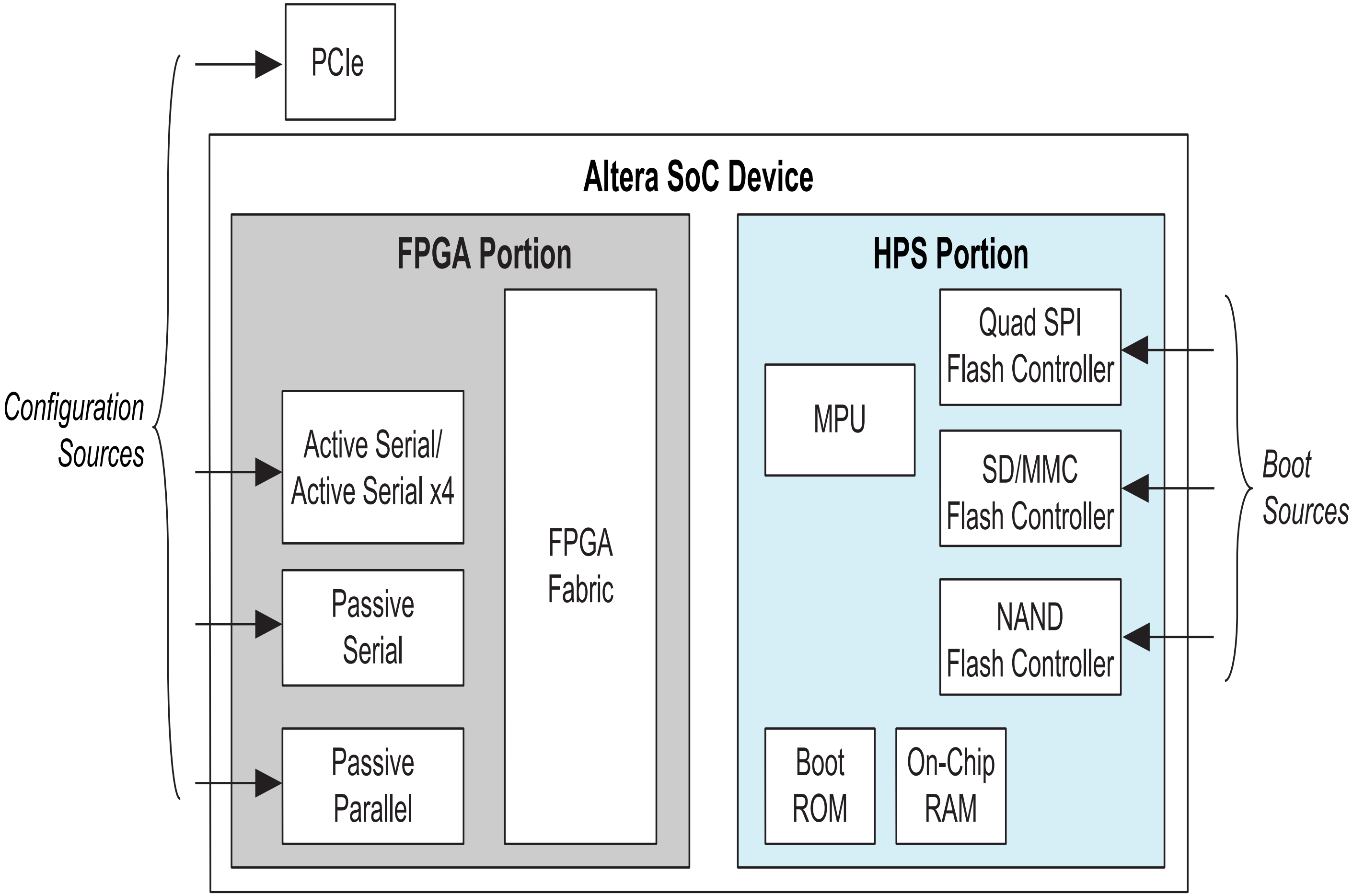


Boot process

- It is possible to use the Cyclone V SoC in 3 different configurations:
  - ➢FPGA-only
  - ➢HPS-only
  - ➢HPS & FPGA
- The configurations using the HPS are more difficult to set up than the *FPGA-only* one.

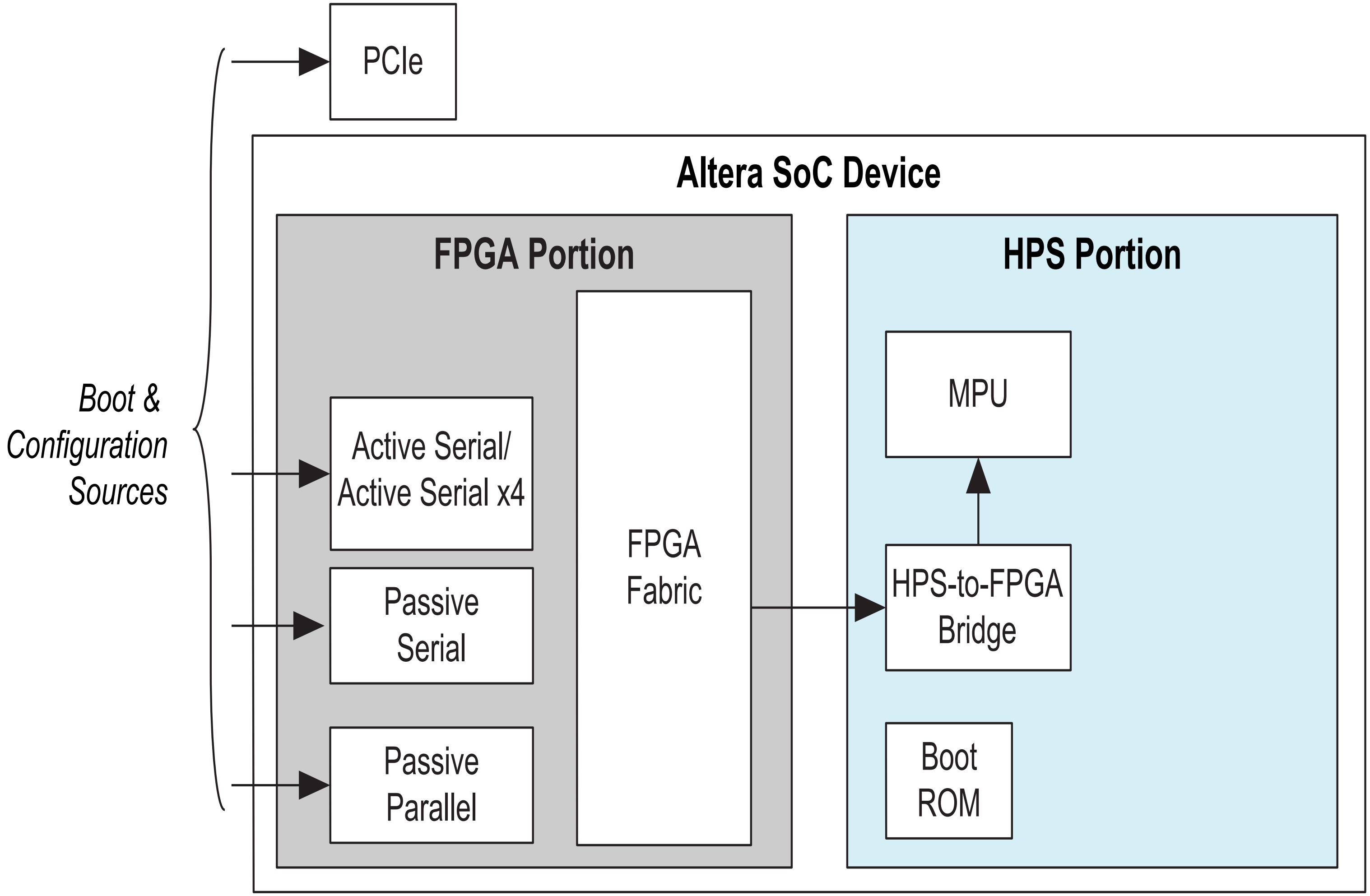
HPS/FPGA Boot (1)

Independent FPGA Configuration and HPS Booting



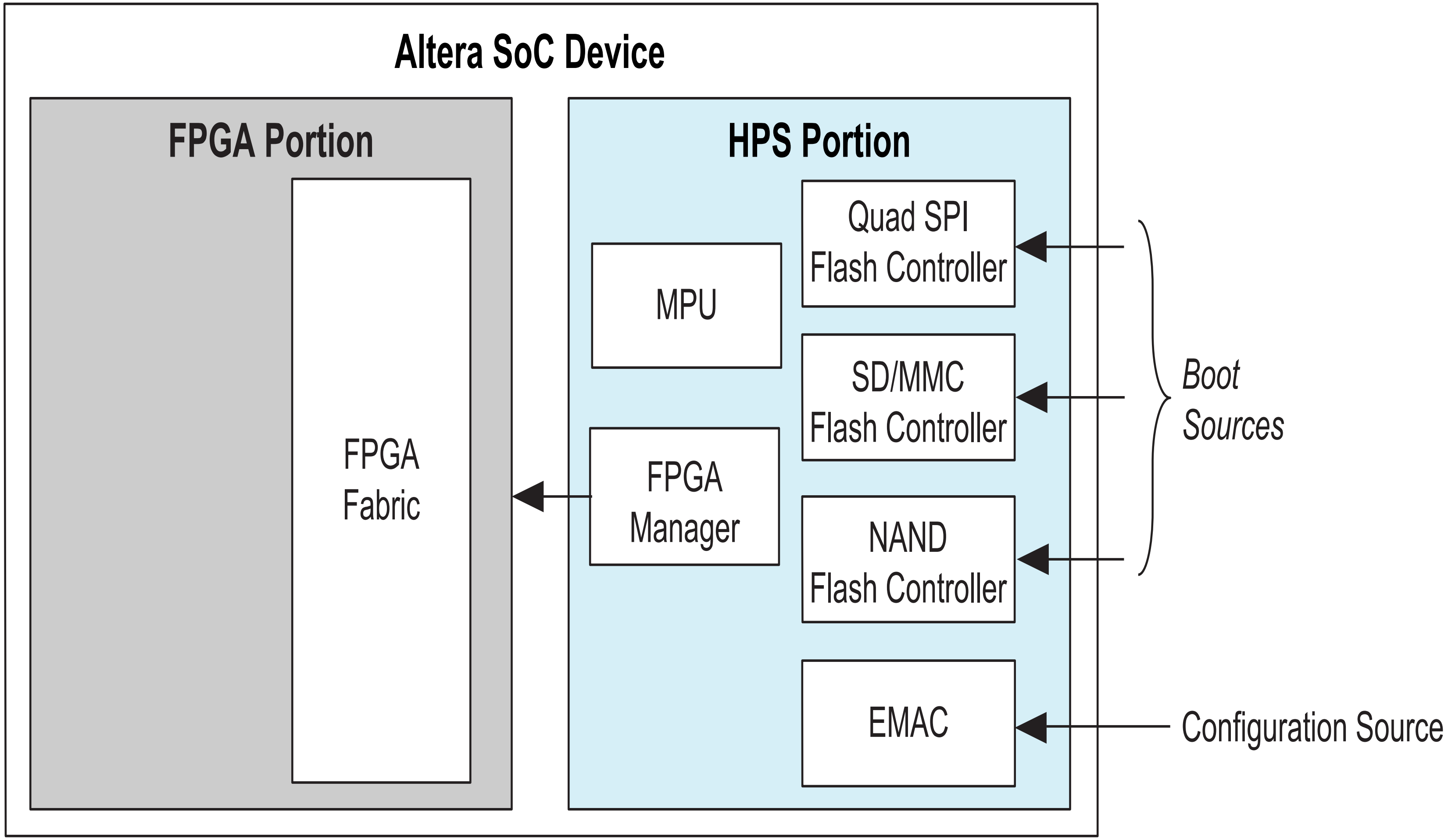
HPS/FPGA Boot (2)

FPGA Configuration before HPS Booting
(HPS boots from FPGA)



HPS/FPGA Boot (3)

HPS Boots and Performs FPGA Configuration



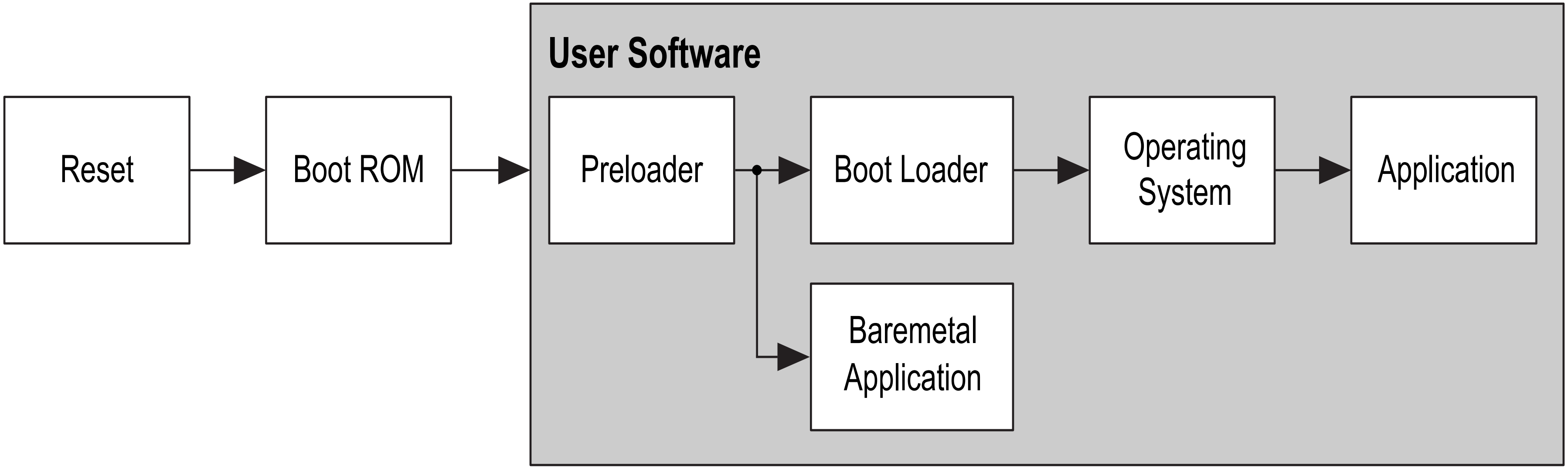
FPGA only case

- Exclusively using the FPGA part of the Cyclone V is easy, as the design process is identical to any other Altera FPGA.
- We can build a complete design in *Quartus II* & *Qsys*, simulate it in *ModelSim-Altera*, then program the FPGA through the *Quartus II Programmer*.
- We can instantiate a Nios II processor in *Qsys,* we can use the *Nios II SBT* IDE to develop software for the processor.

Type of Application

- OS based (ie: Linux)
- Bare-metal (No OS)

HPS Boot Flows



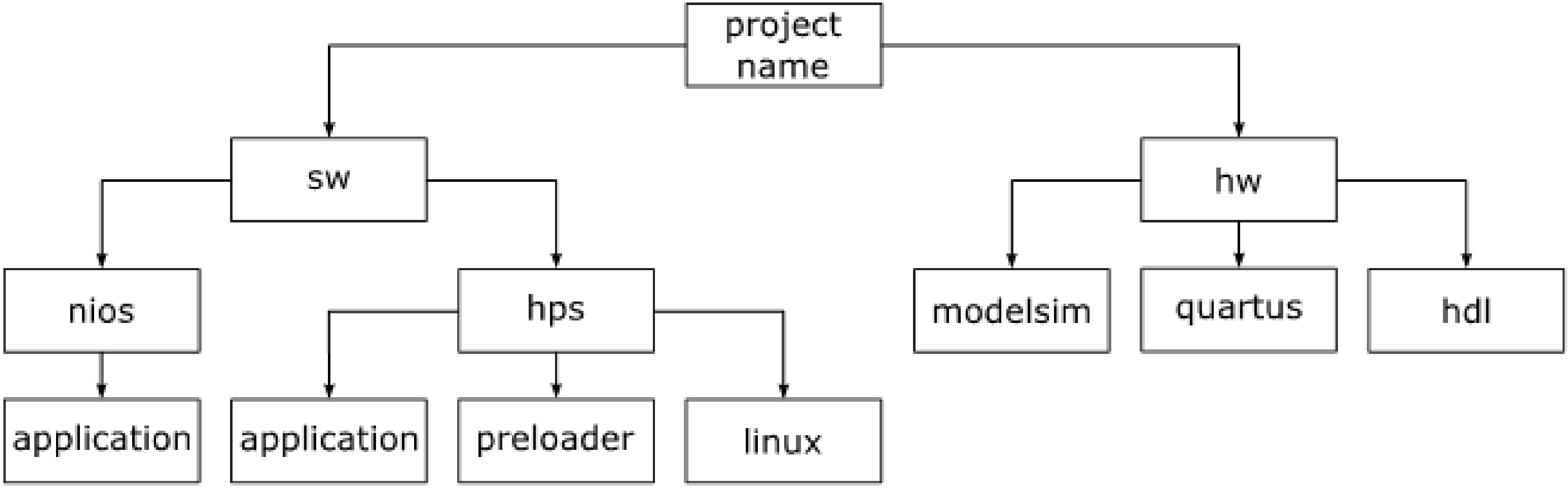
*Although the HPS has a **DUAL**-processor,*
CPU1 is under reset, and the boot flow only executes on CPU0.

If we want to use both processors,
*then **USER SOFTWARE** executing on CPU0 is responsible*
for releasing CPU1 from reset

Preloader

- The preloader is one of the most important boot stages. It is actually what one would call the boot "*source*", as **all stages before it are unmodifiable**. The preloader can be stored on external flash-based memory, or in the FPGA fabric.
- The preloader typically performs the following actions:
  - Initialize the SDRAM interface
  - Configure the HPS I/O through the scan manager
  - Configure pin multiplexing through the system manager
  - Configure HPS clocks through the clock manager
  - Initialize the flash controller (NAND, SD/MMC, QSPI) that contains the next stage boot software
  - Load the next boot software into the SDRAM and pass control to it
- The preloader does ***NOT*** release CPU1 from reset. The subsequent stages of the boot process are responsible for it if they want to use the extra processor.

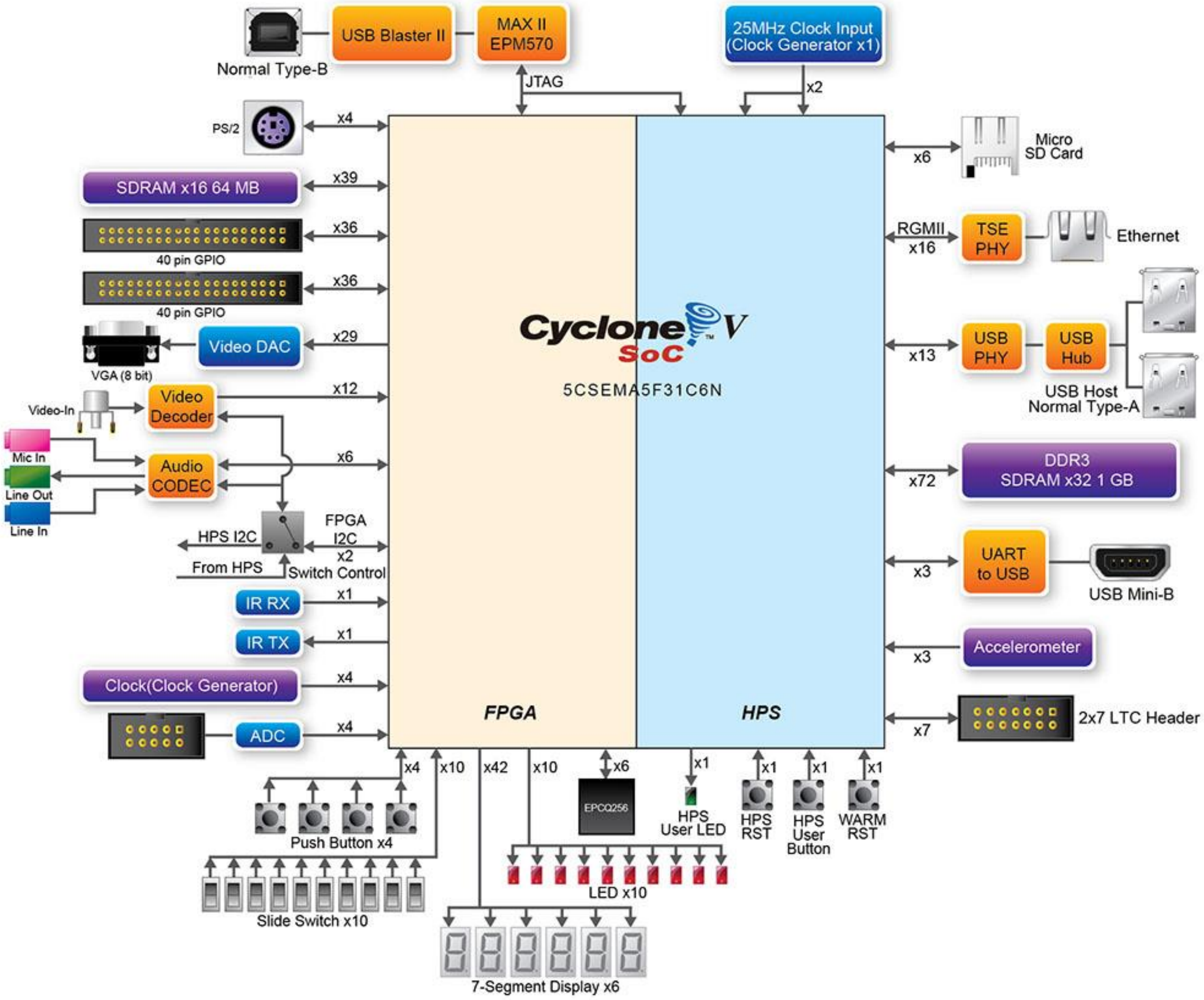
Project structure



DE1-SOC BOARD (TERASIC)

www.terasic.com.tw

DE1-SOC Bloc Diagramm

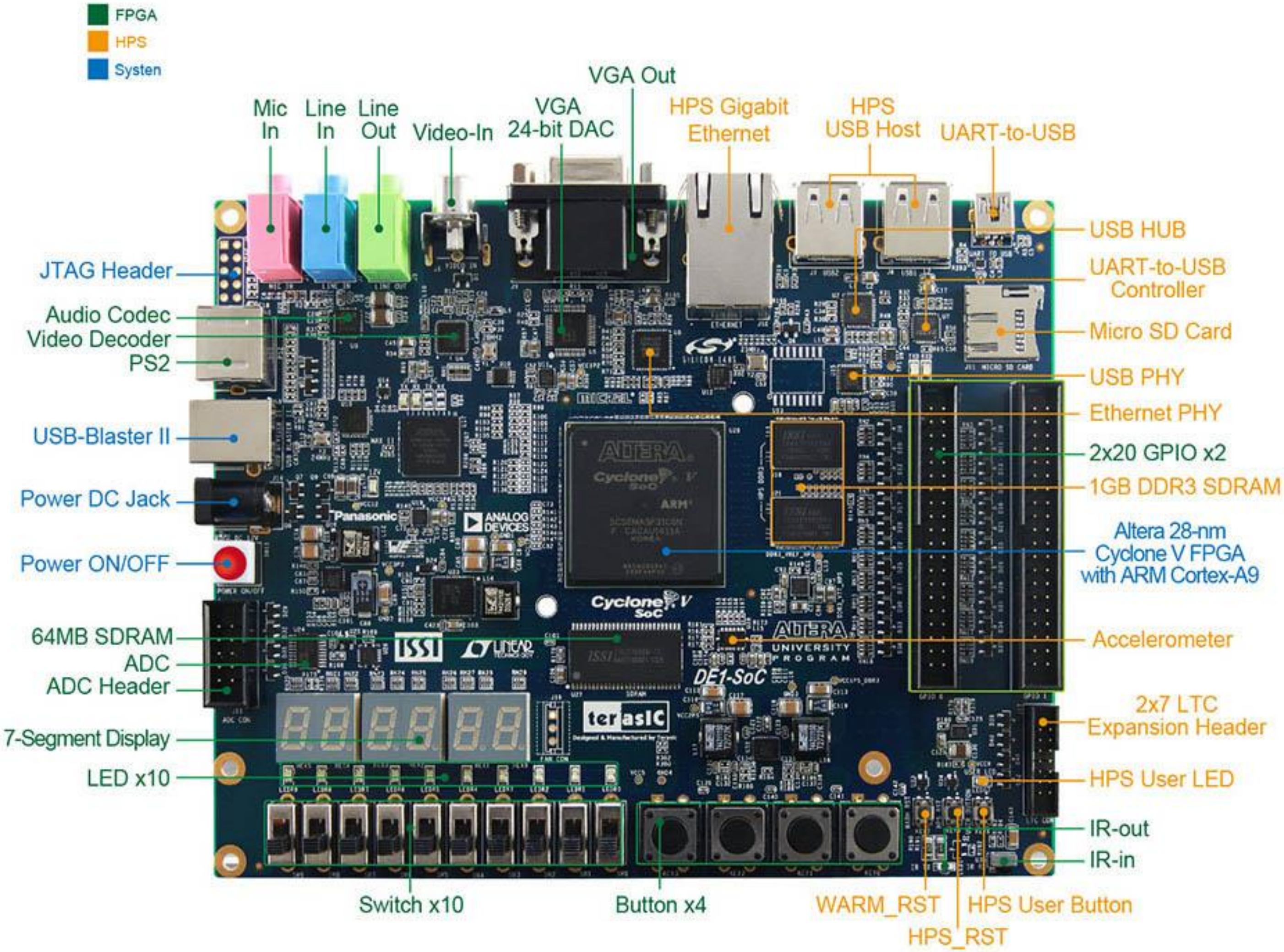


DE1-SoC

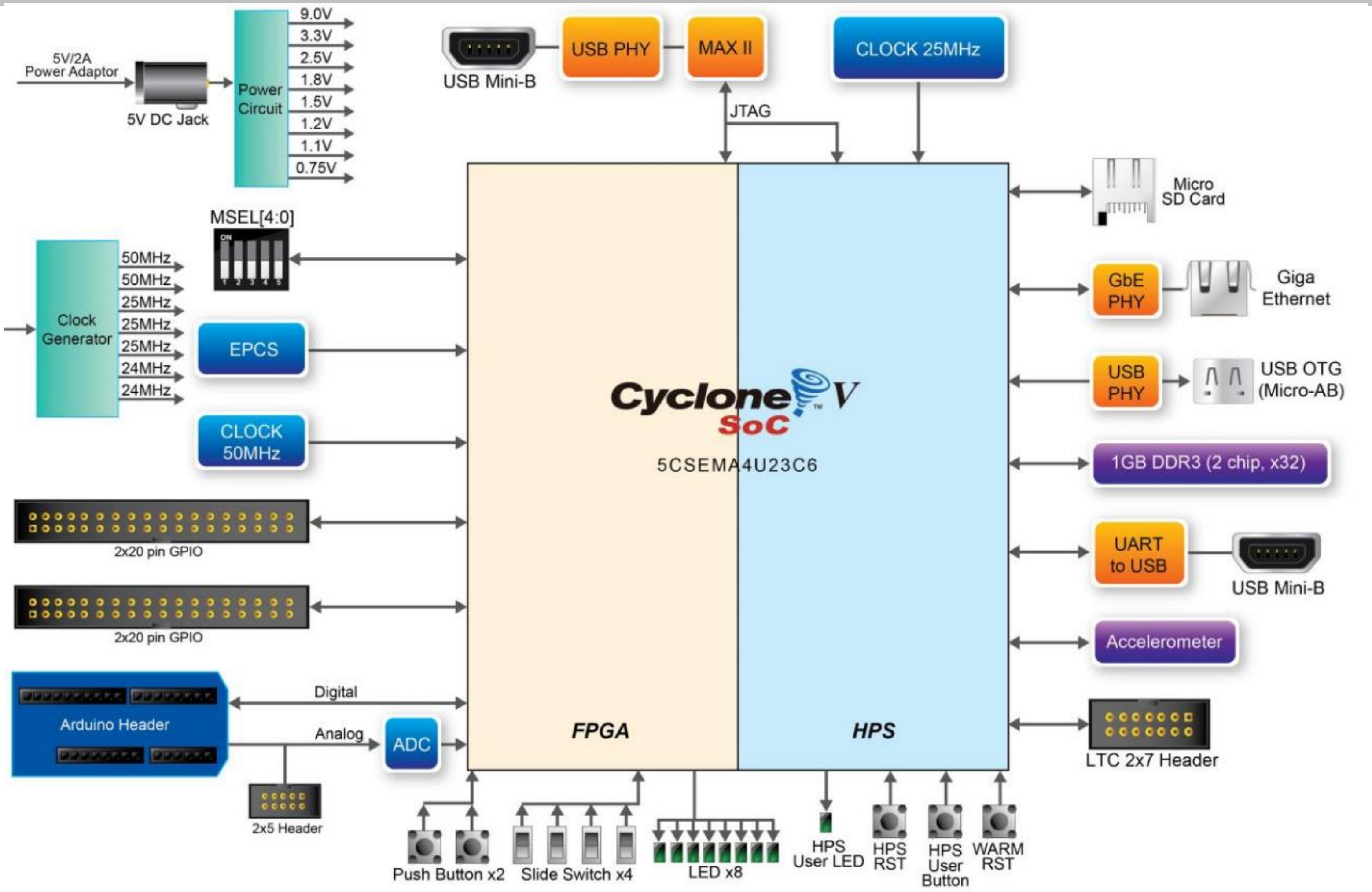
Green for peripherals directly connected to the FPGA

Orange for peripherals directly connected to the HPS

Blue for board control

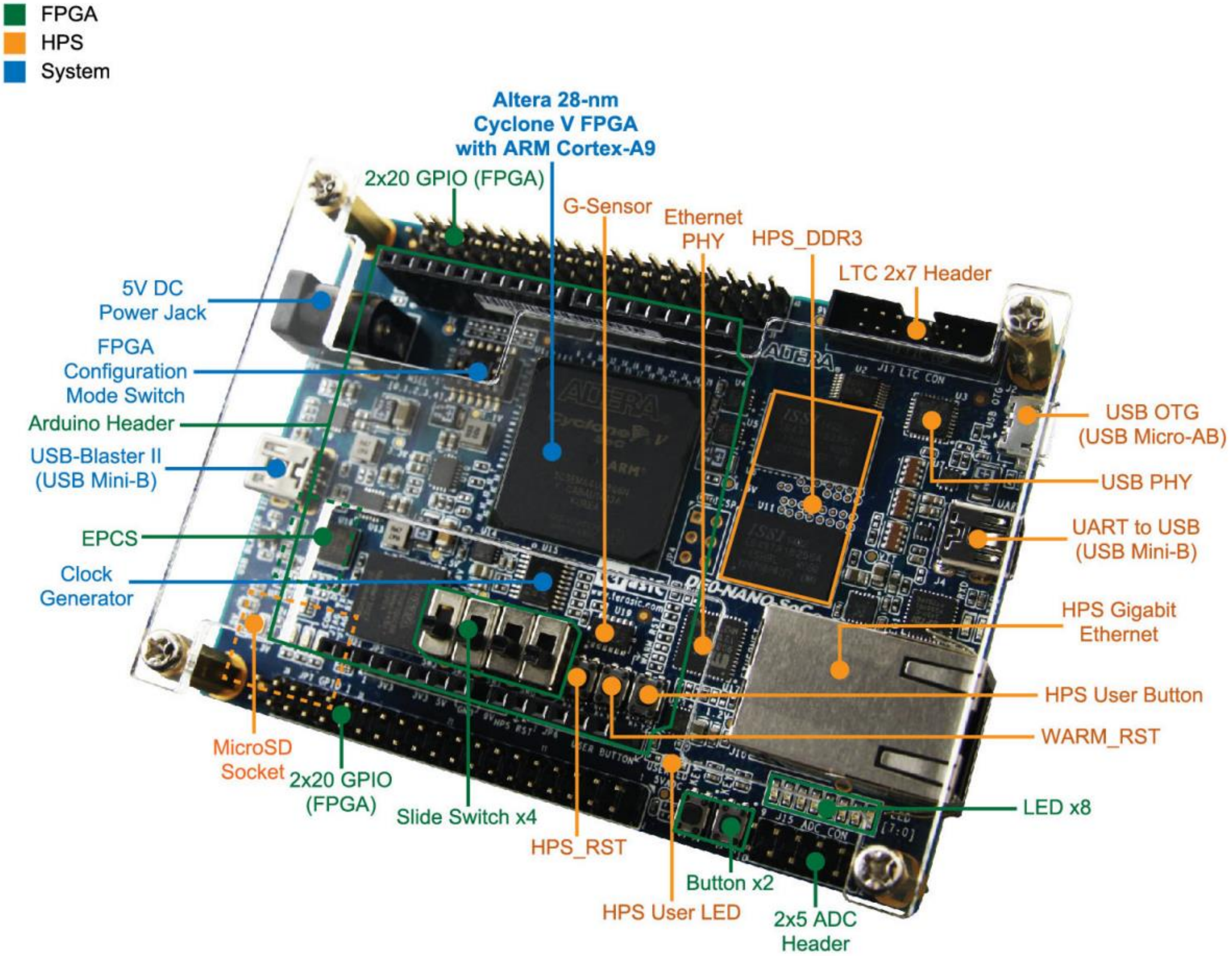


DE0-nano-SoC

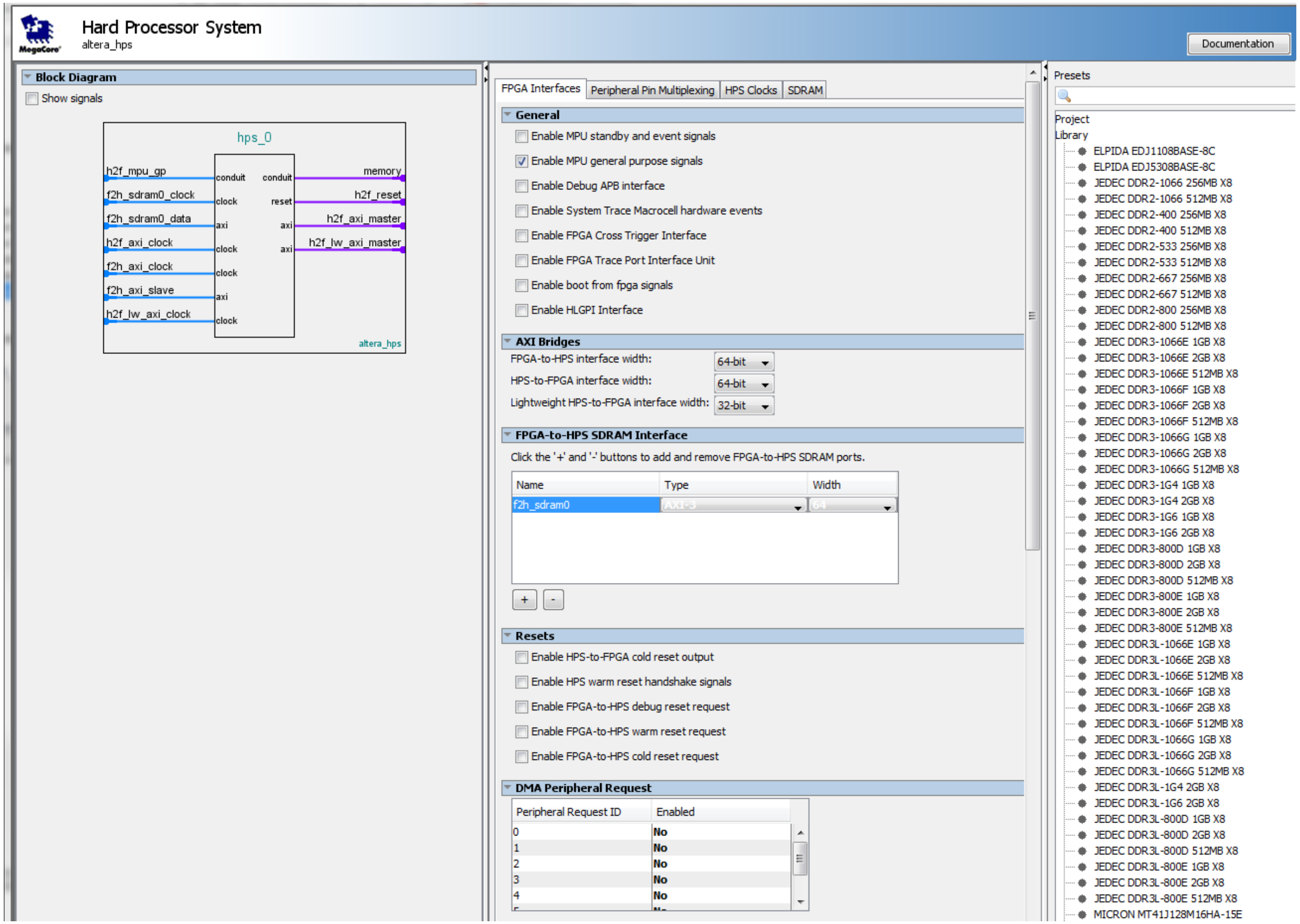


http://www.terasic.com.tw/attachment/archive/941/DE0-Nano-SoC_User_manual_rev.C1.pdf

DE0-nano-SoC


🟩 FPGA
🟧 HPS
🟦 System
Altera 28-nm Cyclone V FPGA with ARM Cortex-A9
2x20 GPIO (FPGA)
G-Sensor
Ethernet PHY
HPS_DDR3
LTC 2x7 Header
5V DC Power Jack
FPGA Configuration Mode Switch
Arduino Header
USB-Blaster II (USB Mini-B)
EPCS
Clock Generator
USB OTG (USB Micro-AB)
USB PHY
UART to USB (USB Mini-B)
HPS Gigabit Ethernet
HPS User Button
WARM_RST
LED x8
MicroSD Socket
2x20 GPIO (FPGA)
Slide Switch x4
HPS_RST
Button x2
HPS User LED
2x5 ADC Header

Qsys, hps definition (1)



Hard Processor System
altera_hps

Block Diagram

□ Show signals

FPGA Interfaces | Peripheral Pin Multiplexing | HPS Clocks | SDRAM

General

- □ Enable MPU standby and event signals
- ☑ Enable MPU general purpose signals
- □ Enable Debug APB interface
- □ Enable System Trace Macrocell hardware events
- □ Enable FPGA Cross Trigger Interface
- □ Enable FPGA Trace Port Interface Unit
- □ Enable boot from fpga signals
- □ Enable HLGPI Interface

AXI Bridges

FPGA-to-HPS interface width: 64-bit

HPS-to-FPGA interface width: 64-bit

Lightweight HPS-to-FPGA interface width: 32-bit

FPGA-to-HPS SDRAM Interface

Click the '+' and '-' buttons to add and remove FPGA-to-HPS SDRAM ports.

Name	Type	Width
f2h_sdram0	AXI-3	64

+ -

Resets

- □ Enable HPS-to-FPGA cold reset output
- □ Enable HPS warm reset handshake signals
- □ Enable FPGA-to-HPS debug reset request
- □ Enable FPGA-to-HPS warm reset request
- □ Enable FPGA-to-HPS cold reset request

DMA Peripheral Request

Peripheral Request ID	Enabled
0	No
1	No
2	No
3	No
4	No

Presets

Project
Library
- ELPIDA EDJ1108BASE-8C
- ELPIDA EDJ5308BASE-8C
- JEDEC DDR2-1066 256MB X8
- JEDEC DDR2-1066 512MB X8
- JEDEC DDR2-400 256MB X8
- JEDEC DDR2-400 512MB X8
- JEDEC DDR2-533 256MB X8
- JEDEC DDR2-533 512MB X8
- JEDEC DDR2-667 256MB X8
- JEDEC DDR2-667 512MB X8
- JEDEC DDR2-800 256MB X8
- JEDEC DDR2-800 512MB X8
- JEDEC DDR3-1066E 1GB X8
- JEDEC DDR3-1066E 2GB X8
- JEDEC DDR3-1066E 512MB X8
- JEDEC DDR3-1066F 1GB X8
- JEDEC DDR3-1066F 2GB X8
- JEDEC DDR3-1066F 512MB X8
- JEDEC DDR3-1066G 1GB X8
- JEDEC DDR3-1066G 2GB X8
- JEDEC DDR3-1066G 512MB X8
- JEDEC DDR3-1G4 1GB X8
- JEDEC DDR3-1G4 2GB X8
- JEDEC DDR3-1G6 1GB X8
- JEDEC DDR3-1G6 2GB X8
- JEDEC DDR3-800D 1GB X8
- JEDEC DDR3-800D 2GB X8
- JEDEC DDR3-800D 512MB X8
- JEDEC DDR3-800E 1GB X8
- JEDEC DDR3-800E 2GB X8
- JEDEC DDR3-800E 512MB X8
- JEDEC DDR3L-1066E 1GB X8
- JEDEC DDR3L-1066E 2GB X8
- JEDEC DDR3L-1066E 512MB X8
- JEDEC DDR3L-1066F 1GB X8
- JEDEC DDR3L-1066F 2GB X8
- JEDEC DDR3L-1066F 512MB X8
- JEDEC DDR3L-1066G 1GB X8
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- JEDEC DDR3L-1066G 512MB X8
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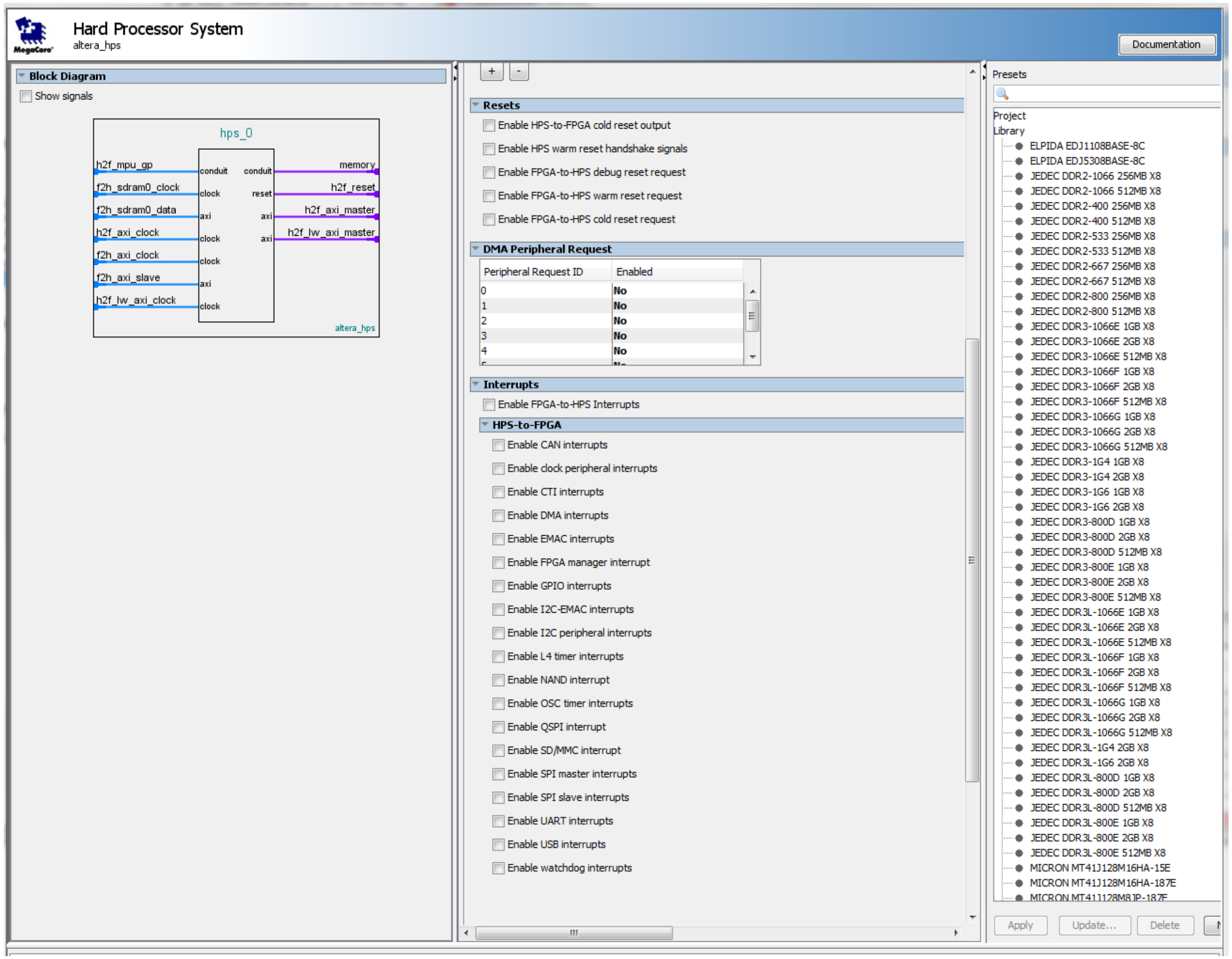
- JEDEC DDR3L-800D 2GB X8
- JEDEC DDR3L-800D 512MB X8
- JEDEC DDR3L-800E 1GB X8
- JEDEC DDR3L-800E 2GB X8
- JEDEC DDR3L-800E 512MB X8
- MICRON MT41J128M16HA-15E

Qsys, hps definition (2)



Hard Processor System
altera_hps

Block Diagram

□ Show signals

Resets

□ Enable HPS-to-FPGA cold reset output
□ Enable HPS warm reset handshake signals
□ Enable FPGA-to-HPS debug reset request
□ Enable FPGA-to-HPS warm reset request
□ Enable FPGA-to-HPS cold reset request

DMA Peripheral Request

Peripheral Request ID	Enabled
0	No
1	No
2	No
3	No
4	No

Interrupts

□ Enable FPGA-to-HPS Interrupts

HPS-to-FPGA

□ Enable CAN interrupts
□ Enable clock peripheral interrupts
□ Enable CTI interrupts
□ Enable DMA interrupts
□ Enable EMAC interrupts
□ Enable FPGA manager interrupt
□ Enable GPIO interrupts
□ Enable I2C-EMAC interrupts
□ Enable I2C peripheral interrupts
□ Enable L4 timer interrupts
□ Enable NAND interrupt
□ Enable OSC timer interrupts
□ Enable QSPI interrupt
□ Enable SD/MMC interrupt
□ Enable SPI master interrupts
□ Enable SPI slave interrupts
□ Enable UART interrupts
□ Enable USB interrupts
□ Enable watchdog interrupts

Presets

Project
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- ELPIDA EDJ1108BASE-8C
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- JEDEC DDR3-1G4 1GB X8
- JEDEC DDR3-1G4 2GB X8
- JEDEC DDR3-1G6 1GB X8
- JEDEC DDR3-1G6 2GB X8
- JEDEC DDR3-800D 1GB X8
- JEDEC DDR3-800D 2GB X8
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- JEDEC DDR3-800E 1GB X8
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- JEDEC DDR3L-800D 512MB X8
- JEDEC DDR3L-800E 1GB X8
- JEDEC DDR3L-800E 2GB X8
- JEDEC DDR3L-800E 512MB X8
- MICRON MT41J128M16HA-15E
- MICRON MT41J128M16HA-187E
- MICRON MT41J128M8JP-187E

IO PIN in HPS

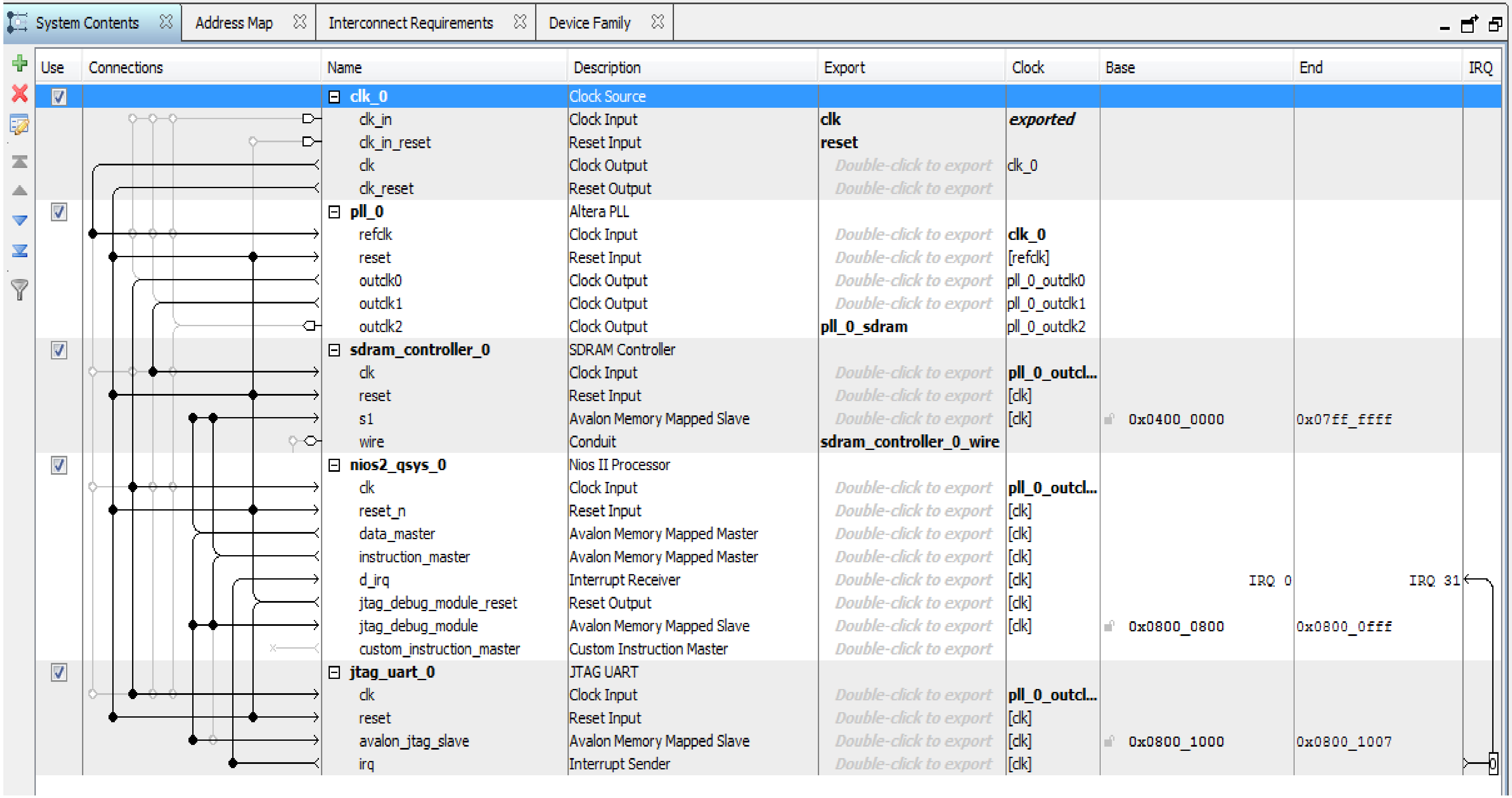
- With the ***PeripheralPin Multiplexing***, some I/O interface can be used by the **HPS part** or the **FPGA part**.
- The selection is done here.

Cyclone V, FPGA development process

For the FPGA part, it’s the same as for the others FPGA, **Quartus II** and **Qsys** tools

- NIOS II processor
- SDRAM Ctrl as softcore module
- Programmable Interface on Avalon Bus
- PLL for Clk and external SDRAM Clk

Cyclone V, FPGA development process

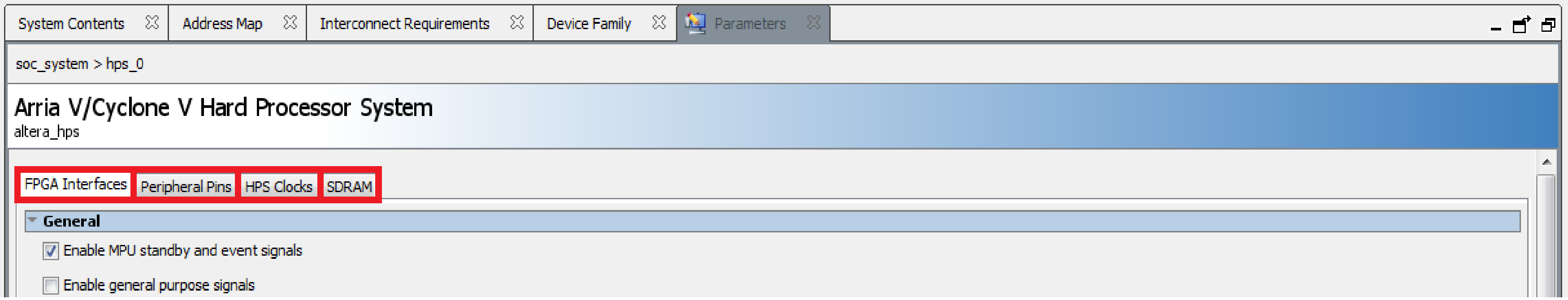


Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
☑		⊟ clk_0	Clock Source					
		clk_in	Clock Input	**clk**	*exported*			
		clk_in_reset	Reset Input	**reset**				
		clk	Clock Output	*Double-click to export*	clk_0			
		clk_reset	Reset Output	*Double-click to export*				
☑		⊟ pll_0	Altera PLL					
		refclk	Clock Input	*Double-click to export*	**clk_0**			
		reset	Reset Input	*Double-click to export*	[refclk]			
		outclk0	Clock Output	*Double-click to export*	pll_0_outclk0			
		outclk1	Clock Output	*Double-click to export*	pll_0_outclk1			
		outclk2	Clock Output	**pll_0_sdram**	pll_0_outclk2			
☑		⊟ sdram_controller_0	SDRAM Controller					
		clk	Clock Input	*Double-click to export*	**pll_0_outcl...**			
		reset	Reset Input	*Double-click to export*	[clk]			
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x0400_0000	0x07ff_ffff	
		wire	Conduit	**sdram_controller_0_wire**				
☑		⊟ nios2_qsys_0	Nios II Processor					
		clk	Clock Input	*Double-click to export*	**pll_0_outcl...**			
		reset_n	Reset Input	*Double-click to export*	[clk]			
		data_master	Avalon Memory Mapped Master	*Double-click to export*	[clk]			
		instruction_master	Avalon Memory Mapped Master	*Double-click to export*	[clk]			
		d_irq	Interrupt Receiver	*Double-click to export*	[clk]	IRQ 0	IRQ 31	
		jtag_debug_module_reset	Reset Output	*Double-click to export*	[clk]			
		jtag_debug_module	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x0800_0800	0x0800_0fff	
		custom_instruction_master	Custom Instruction Master	*Double-click to export*				
☑		⊟ jtag_uart_0	JTAG UART					
		clk	Clock Input	*Double-click to export*	**pll_0_outcl...**			
		reset	Reset Input	*Double-click to export*	[clk]			
		avalon_jtag_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x0800_1000	0x0800_1007	
		irq	Interrupt Sender	*Double-click to export*	[clk]			0

Cyclone V, HPS development process

For the HPS part, it's the same as for the others FPGA, **Quartus II** and **Qsys** tools

- HPS configuration with Qsys
- I/O pins association



soc_system > hps_0

Arria V/Cyclone V Hard Processor System

altera_hps

General

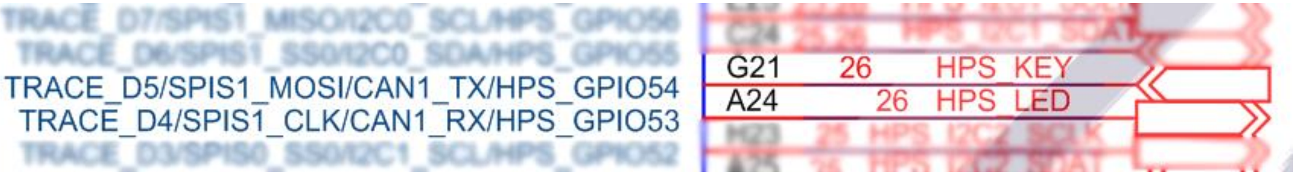
☑ Enable MPU standby and event signals

□ Enable general purpose signals

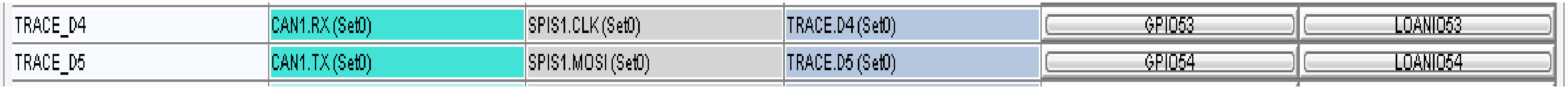
Cyclone V, HPS I/O selection

Ex.: **HPS_KEY** & **HPS_LED**

From schematics:

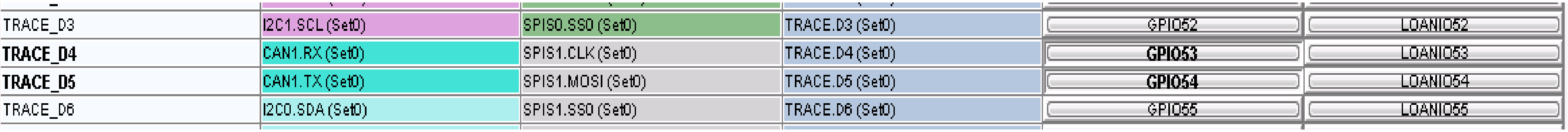

TRACE_D7/SPIS1_MISO/I2C0_SCL/HPS_GPIO56
TRACE_D6/SPIS1_SS0/I2C0_SDA/HPS_GPIO55
TRACE_D5/SPIS1_MOSI/CAN1_TX/HPS_GPIO54
TRACE_D4/SPIS1_CLK/CAN1_RX/HPS_GPIO53
TRACE_D3/SPIS0_SS0/I2C1_SCL/HPS_GPIO52
C24 25,26 HPS_I2C1_SDAT
G21 26 HPS_KEY
A24 26 HPS_LED
H23 25 HPS_I2C2_SCLK
A25 26 HPS_I2C2_SDAT

In Qsys selection for the specifics pins:



TRACE_D4	CAN1.RX (Set0)	SPIS1.CLK (Set0)	TRACE.D4 (Set0)	GPIO53	LOANIO53
TRACE_D5	CAN1.TX (Set0)	SPIS1.MOSI (Set0)	TRACE.D5 (Set0)	GPIO54	LOANIO54

Mode GPIO:

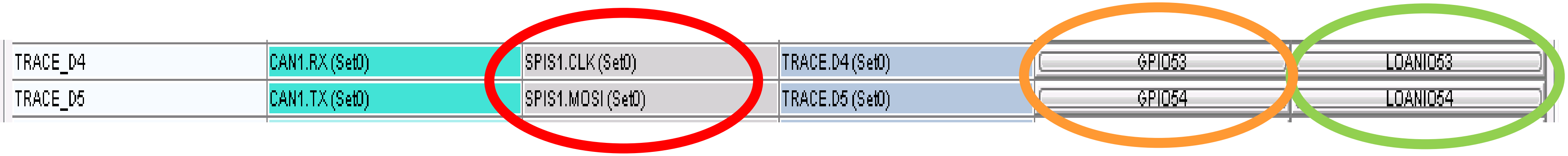


TRACE_D3	I2C1.SCL (Set0)	SPIS0.SS0 (Set0)	TRACE.D3 (Set0)	GPIO52	LOANIO52
TRACE_D4	CAN1.RX (Set0)	SPIS1.CLK (Set0)	TRACE.D4 (Set0)	**GPIO53**	LOANIO53
TRACE_D5	CAN1.TX (Set0)	SPIS1.MOSI (Set0)	TRACE.D5 (Set0)	**GPIO54**	LOANIO54
TRACE_D6	I2C0.SDA (Set0)	SPIS1.SS0 (Set0)	TRACE.D6 (Set0)	GPIO55	LOANIO55

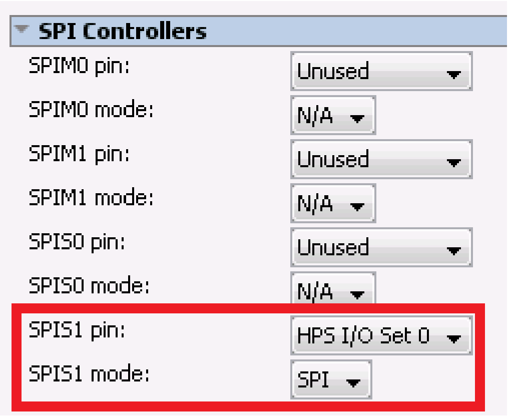
Cyclone V, HPS I/O selection

Ex.: **HPS_KEY** & **HPS_LED**

- ***GPIO****XY*: Configures the pin to be connected to the ***HPS' GPIO*** peripheral.



TRACE_D4	CAN1.RX (Set0)	SPIS1.CLK (Set0)	TRACE.D4 (Set0)	GPIO53	LOANIO53
TRACE_D5	CAN1.TX (Set0)	SPIS1.MOSI (Set0)	TRACE.D5 (Set0)	GPIO54	LOANIO54

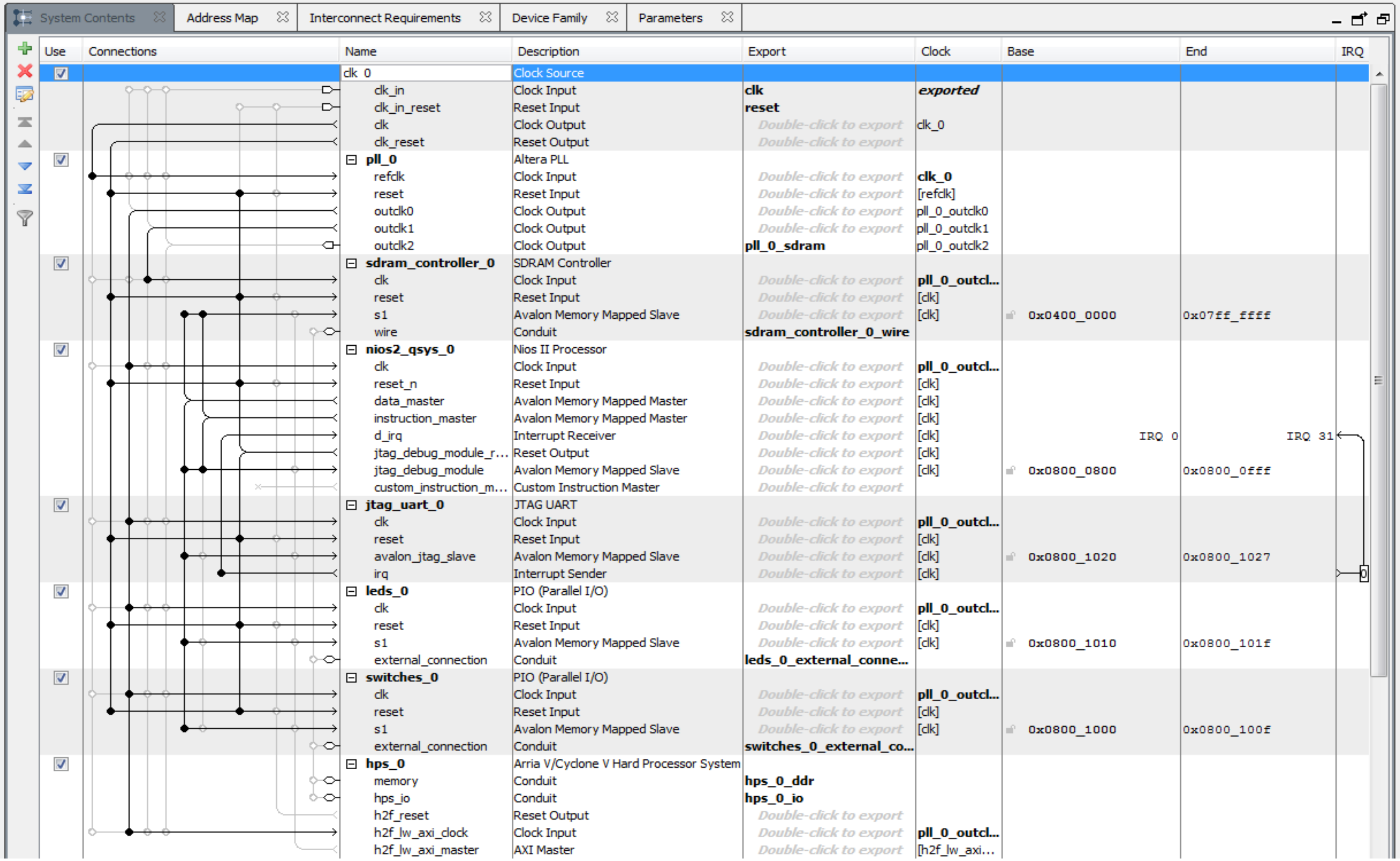


SPI Controllers

SPIM0 pin:	Unused
SPIM0 mode:	N/A
SPIM1 pin:	Unused
SPIM1 mode:	N/A
SPIS0 pin:	Unused
SPIS0 mode:	N/A
SPIS1 pin:	HPS I/O Set 0
SPIS1 mode:	SPI

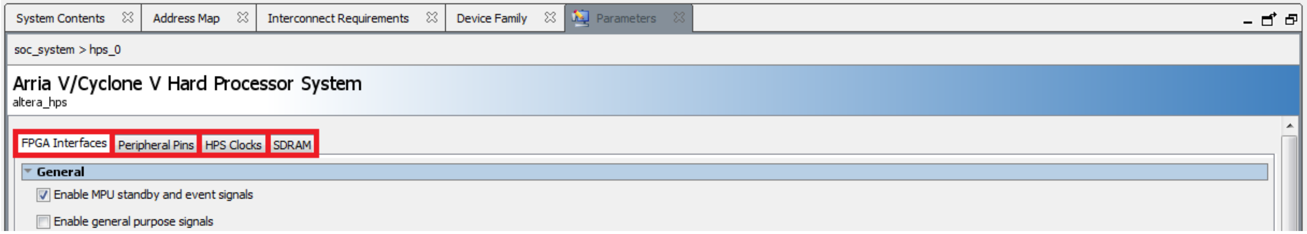
- ***LOANIO****XY*: Configures the pin to be connected to the ***FPGA*** fabric. This pin can be exported from *Qsys* to be used by the FPGA.

Cyclone V, HPS – FPGA development process



Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
☑		clk_0	Clock Source					
		clk_in	Clock Input	clk	exported			
		clk_in_reset	Reset Input	reset				
		clk	Clock Output	Double-click to export	clk_0			
		clk_reset	Reset Output	Double-click to export				
☑		⊟ pll_0	Altera PLL					
		refclk	Clock Input	Double-click to export	clk_0			
		reset	Reset Input	Double-click to export	[refclk]			
		outclk0	Clock Output	Double-click to export	pll_0_outclk0			
		outclk1	Clock Output	Double-click to export	pll_0_outclk1			
		outclk2	Clock Output	pll_0_sdram	pll_0_outclk2			
☑		⊟ sdram_controller_0	SDRAM Controller					
		clk	Clock Input	Double-click to export	pll_0_outcl...			
		reset	Reset Input	Double-click to export	[clk]			
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x0400_0000	0x07ff_ffff	
		wire	Conduit	sdram_controller_0_wire				
☑		⊟ nios2_qsys_0	Nios II Processor					
		clk	Clock Input	Double-click to export	pll_0_outcl...			
		reset_n	Reset Input	Double-click to export	[clk]			
		data_master	Avalon Memory Mapped Master	Double-click to export	[clk]			
		instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]			
		d_irq	Interrupt Receiver	Double-click to export	[clk]	IRQ 0	IRQ 31	
		jtag_debug_module_r...	Reset Output	Double-click to export	[clk]			
		jtag_debug_module	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x0800_0800	0x0800_0fff	
		custom_instruction_m...	Custom Instruction Master	Double-click to export				
☑		⊟ jtag_uart_0	JTAG UART					
		clk	Clock Input	Double-click to export	pll_0_outcl...			
		reset	Reset Input	Double-click to export	[clk]			
		avalon_jtag_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x0800_1020	0x0800_1027	
		irq	Interrupt Sender	Double-click to export	[clk]			0
☑		⊟ leds_0	PIO (Parallel I/O)					
		clk	Clock Input	Double-click to export	pll_0_outcl...			
		reset	Reset Input	Double-click to export	[clk]			
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x0800_1010	0x0800_101f	
		external_connection	Conduit	leds_0_external_conne...				
☑		⊟ switches_0	PIO (Parallel I/O)					
		clk	Clock Input	Double-click to export	pll_0_outcl...			
		reset	Reset Input	Double-click to export	[clk]			
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x0800_1000	0x0800_100f	
		external_connection	Conduit	switches_0_external_co...				
☑		⊟ hps_0	Arria V/Cyclone V Hard Processor System					
		memory	Conduit	hps_0_ddr				
		hps_io	Conduit	hps_0_io				
		h2f_reset	Reset Output	Double-click to export				
		h2f_lw_axi_clock	Clock Input	Double-click to export	pll_0_outcl...			
		h2f_lw_axi_master	AXI Master	Double-click to export	[h2f_lw_axi...			

Cyclone V, HPS – DDR3 configuration


System Contents | Address Map | Interconnect Requirements | Device Family | Parameters

soc_system > hps_0

Arria V/Cyclone V Hard Processor System
altera_hps

FPGA Interfaces | Peripheral Pins | HPS Clocks | SDRAM

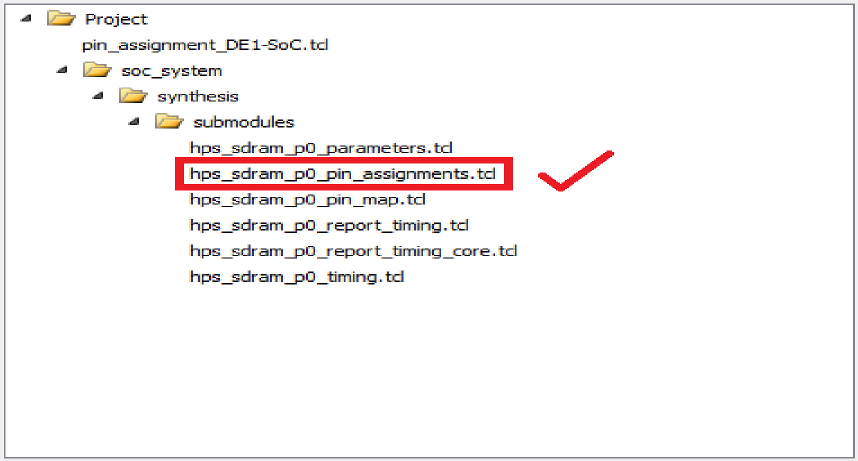
General

☑ Enable MPU standby and event signals

☐ Enable general purpose signals

SDRAM Tab:

- In fact DDR3 memories
- Put the right parameters
- Assign the pins with tcl file


```
Project
    pin_assignment_DE1-SoC.tcl
    soc_system
        synthesis
            submodules
                hps_sdram_p0_parameters.tcl
                hps_sdram_p0_pin_assignments.tcl
                hps_sdram_p0_pin_map.tcl
                hps_sdram_p0_report_timing.tcl
                hps_sdram_p0_report_timing_core.tcl
                hps_sdram_p0_timing.tcl
```

Exercises / Mini Project

1. Use the DE1-SOC/DE0-nano-SoC without the ARM-A9
   - NIOS design to access the Switches and LEDs
   - Adapt the LCD/camera controller for the NIOSII

2. Use the ARM-A9 with ARM DS-5 software
   - Access through the AXI bridge the Avalon part of the FPGA
   - Control the LCD/camera from the ARM

- Try the Linux access of the FPGA…to control LCD and Camera
- In option !